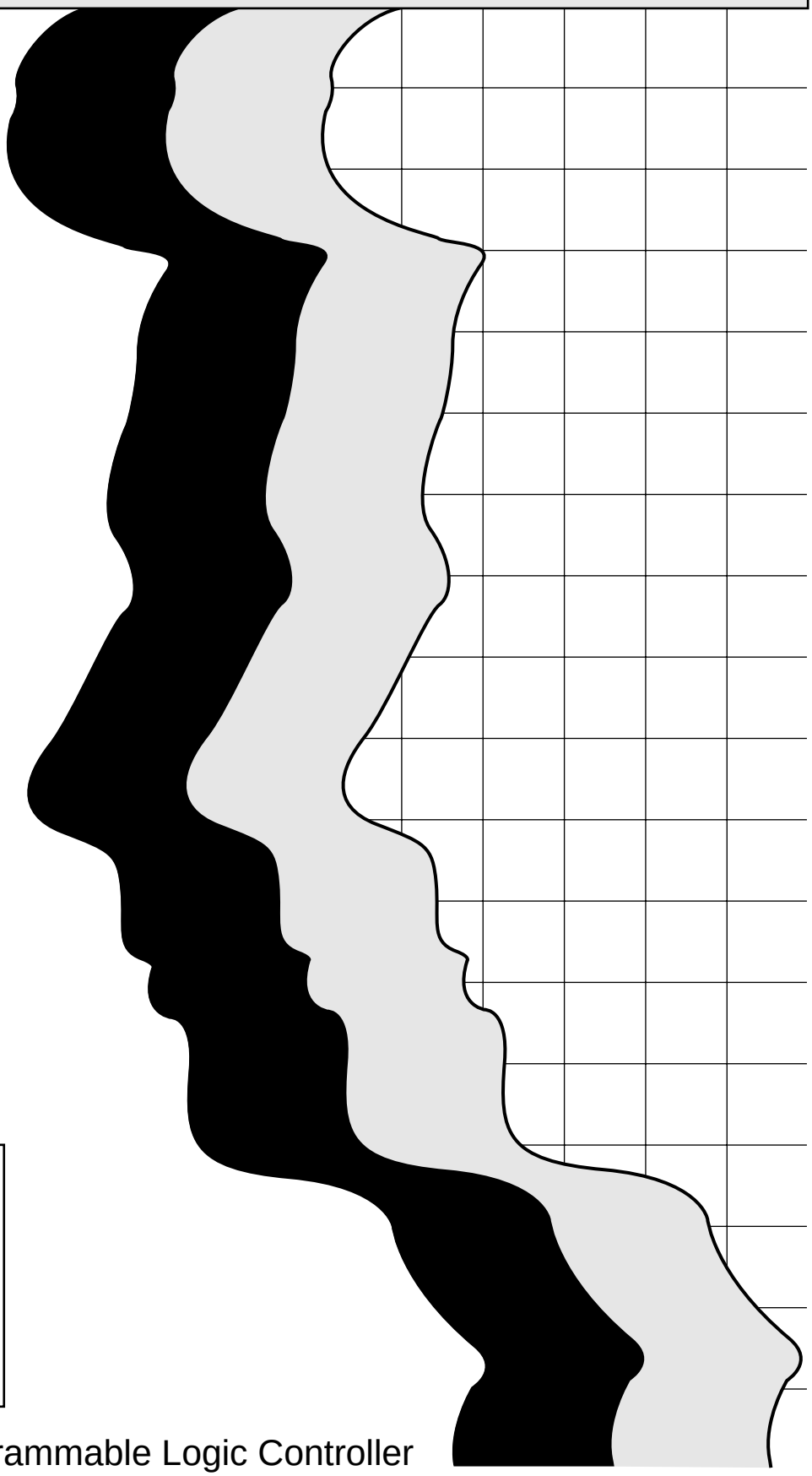
MITSUBISHI

Analog-Digital Converter Module type A68ADN

User's Manual



A

MELSEC

Mitsubishi Programmable Logic Controller

● SAFETY PRECAUTIONS ●

(Always read these instructions before using this equipment.)

Before using this product, please read this manual and the relevant manuals introduced in this manual carefully and pay full attention to safety to handle the product correctly.
The instructions given in this manual are concerned with this product. Refer to the User's Manual of the CPU module in use for details on the safety instructions for the programmable logic controller system.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

⚠ DANGER	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠ CAUTION	Indicates that incorrect handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage.

Note that the ⚠ **CAUTION** level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please save this manual to make it accessible when required and always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- **Do not write data into the "system area" of the buffer memory of intelligent function modules.**
  Also, do not use any "prohibited to use" signals as an output signal to an intelligent function module from the PLC CPU.
  Writing data into the "system area" or outputting a signal for "prohibited to use" may cause a PLC system malfunction.

⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 100mm (3.94inch) or more from each other.
  Not doing so could result in noise that would cause erroneous operation.

[INSTALLATION PRECAUTIONS]

⚠ CAUTION

- Use the PLC in an environment that meets the general specifications given in the User's Manual of the CPU module in use.
  Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.
- Securely insert the module fixing latch on the module bottom into the fixing holes on the base unit before mounting. Incorrect mounting of the module could lead to erroneous operation, faults or drop.
- Tighten the screws within the range of specified torque.
  If the screws are loose, it may cause the module to fallout, short circuits, or malfunction.
  If the screws are tightened too much, it may cause damage to the screw and/or the module, resulting in fallout, short circuits or malfunction.
- Switch all phases of the external power supply off when mounting or removing the module.
  Not doing so may cause damage to the module.
- Do not directly touch the module's conductive parts or electronic components.
  Touching the conductive parts could cause an operation failure or give damage to the module.

[WIRING PRECAUTIONS]

⚠ CAUTION

- Ground the AG terminal and FG terminal with grounding dedicated for the PLC, especially when there are high levels of noise.
  Failure to observe this could lead to erroneous operation.
- When turning on the power and operating the module after wiring is completed, always attach the terminal cover that comes with the product.
  There is a risk of electric shock if the terminal cover is not attached.
- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, or erroneous operation.
  If the terminal screws tightened too tight, it may cause damage to the screw and/or the module, resulting in short circuits or malfunction.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module.
  Such debris could cause fires, damage, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠ CAUTION

- **Do not disassemble or modify the module.**
  This may result in failure, malfunction, injury or fire.
- **Be sure to externally shut all power phases off before mounting or removing the module.**
  Failure to observe this may cause the module to fail or malfunction.
- **Do not touch the terminals during conduction.**
  This may result in malfunction.
- **Be sure to externally shut all power phases off before cleaning or retightening the terminal screws and module mounting screw.**
  Failure to externally shut all power phases off may cause the module to fail or malfunction.
  If the screws are loose, it may cause fallout, short circuits, or malfunction.
  If the screws are tightened too much, it may damage the screw and/or the module, resulting in fallout, short circuits or malfunction.

[DISPOSAL PRECAUTIONS]

⚠ CAUTION

- When disposing of the product, handle it as industrial waste.

REVISIONS

*The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
Jul., 1991	IB(NA)66307-A	First edition
May, 2000	IB(NA)66307-B	Addition WARRANTY Part Addition 3.3.3 Correction SAFETY PRECAUTIONS, CONTENTS, Section 2.2, 3.1, 3.2, 3.3.2, 4.1, 4.2, 4.4.2, 5.1, 5.3, APPENDICES2
June, 2002	IB(NA)66307-C	Part Addition SAFETY PRECAUTIONS, Section 2.1, 2.2, 3.1, 3.2, 4.4.2, 5.3

Japanese Manual Version IB-68219-F

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series Programmable Logic Controllers. Please read this manual carefully so that the equipment is used to its optimum.
A copy of this manual should be forwarded to the end User.

CONTENTS

1. INTRODUCTION

This manual gives specifications, handling, programming procedures, etc. for the A68ADN analog-digital converter module (hereafter referred to as the A68ADN) when used with MELSEC-A series PC CPU modules.

An A68ADN converts analog signals (voltage or current) into 16-bits, signed binary digital values, as shown in the following figure.

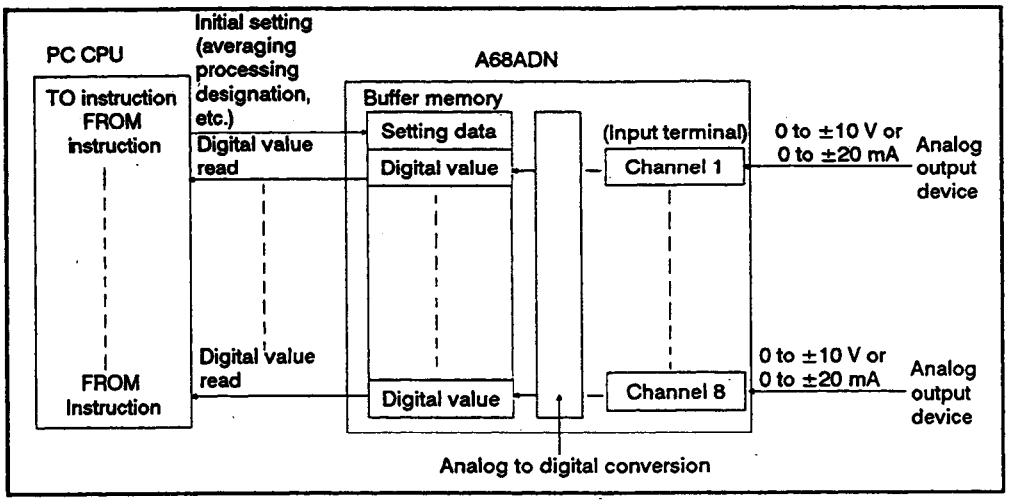


Figure 1.1 Analog to Digital Conversion

A chart showing differences between the A68ADN and the A68AD, A68AD-S2, and A616AD is given in Appendix 1.

1.1 Features

(1) 8 channels for analog to digital (here in after A-D) conversion.

The A616ADN converts A-D for eight channels in one complete operation. Voltage or current input can be selected for each channel.

(2) 1/12000 high resolution (all channels)

Resolution is selectable from 1/4000, 1/8000, and 1/12000. High resolution digital values can be obtained. Resolution setting applies to all channels.

(3) Averaging processing by specifying time or frequency (for each channel)

In addition to sampling processing (in which the digital value obtained in A-D conversion is output for each A-D conversion) averaging processing is available in a specified time or frequency.
The A-D conversion mode is selectable for each channel.

(4) Conversion enable/disable setting (for each channel)

Whether A-D conversion is enabled or disabled can be set for each channel. By setting "disable" for the unused channels, conversion speed can be increased.

(5) Offset/gain adjustment without dials (for each channel)

Offset and gain can be set by simply inputting the required value (voltage or current) and turning the setting switch ON.

2. SYSTEM CONFIGURATIONS

2.1 Overall Configurations

(1) Figure 2.1 shows the overall system configuration when the A68ADN is used with a building block-type PC CPU

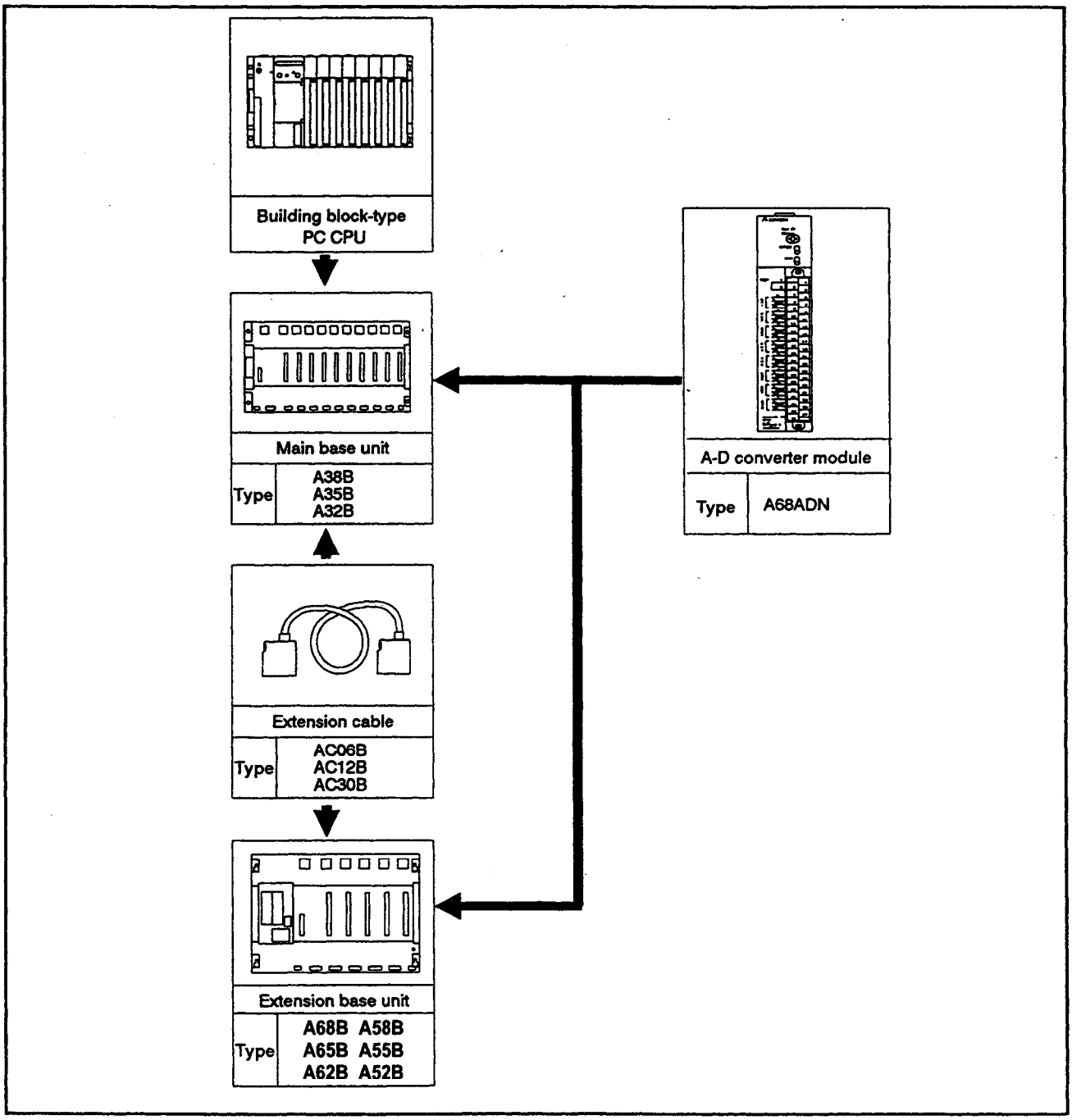


Fig.2.1 Overall Configuration Using a Building Block-Type PC CPU

(2) Figure 2.2 shows the overall system configuration when the A68ADN is used with a compact-type PC CPU

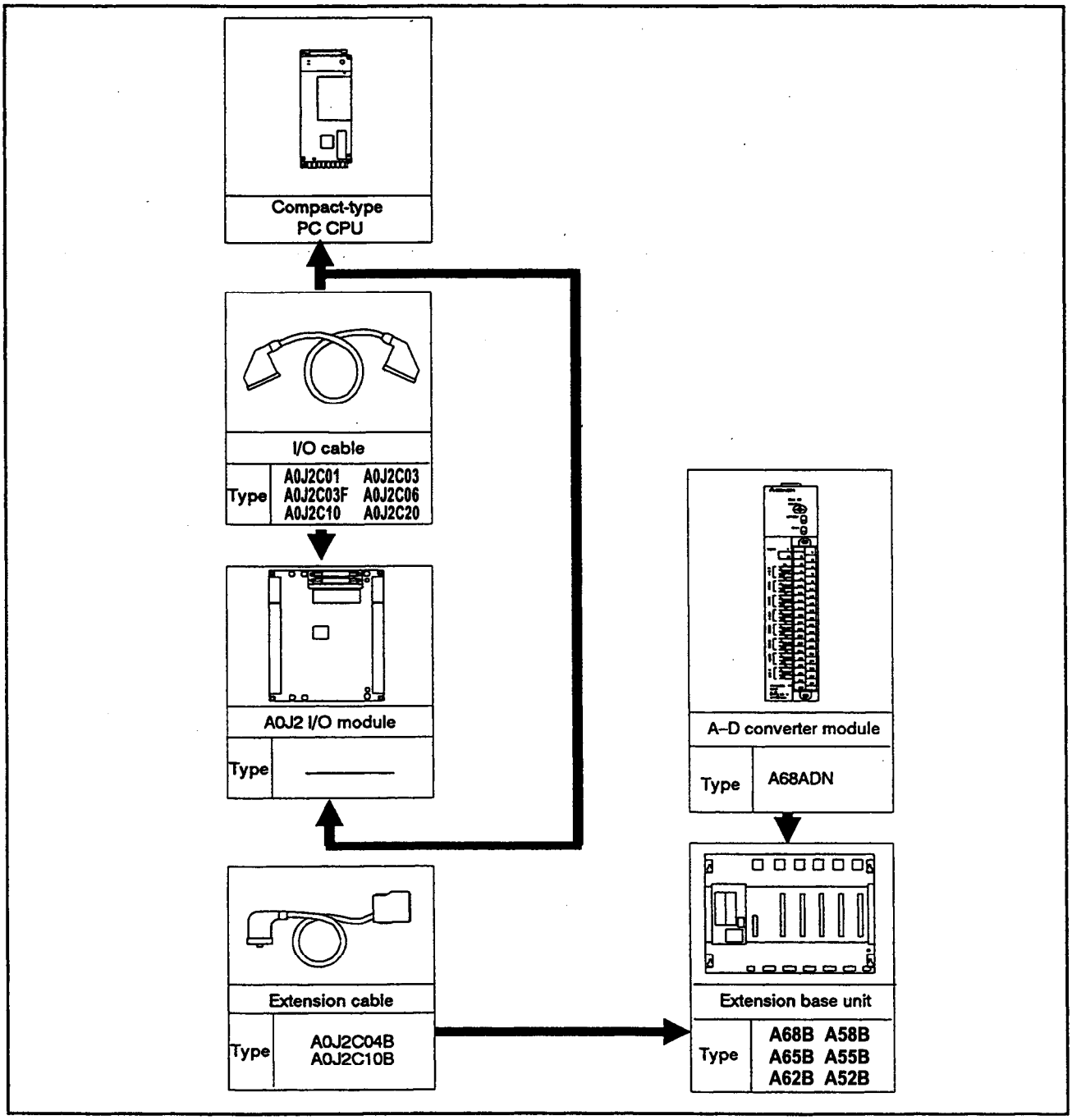


Fig. 2.2 Overall Configuration Using a Compact-Type PC CPU

2.2 Applicable Systems

(1) The following PC CPU modules and remote I/O module are compatible with an A68ADN:

Applicable models

A0J2CPU (P21/R21)	AOJ2CPU (P23/R23)	
A1NCPU (P21/R21)	A1CPU (P21/R21)	
A2NCPU (P21/R21)	A2CPU (P21/R21)	A2ACPU (P21/R21)
A2NCPU (P21/R21)-S1	A2CPU (P21/R21)-S1	A2ACPU (P21/R21)-S1
A3NCPU (P21/R21)	A3CPU (P21/R21)	A3ACPU (P21/R21)
A3HCPU (P21/R21)	Q2ACPU	A2UCPU
A3MCPU (P21/R21)	Q2ACPU-S1	A2UCPU-S1
A73CPU (P21/R21)	Q3ACPU	A3UCPU
A81CPU	Q4ACPU	A4UCPU
	Q4ARCPU	

Applicable remote I/O

AJ71P25/R25

POINT

The A68ADN is not compatible with the A0J2P25/R25 (remote I/O station)

(2) Attach the A68ADN to any slot of the base unit considering following:

It is not recommended to mount A68ADN to A52B, A55B or A58B extension base unit on which no power supply module is mounted, since it may lead to insufficient current capacity.
If the above configuration is required, select the suitable power supply module and extension cable considering the current capacity of power supply module and voltage drop of extension cable

Refer to the User's Manual of the PC CPU module for details.

3. SPECIFICATIONS

3.1 General Specifications

The following table shows the general specifications of the A68ADN.

Table 3.1 General Specifications

<table>
<tr><th>Item</th><th colspan="6">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="6">0 to 55°C</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="6">–20 to 75°C</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="6">10 to 90%RH, No condensation</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="6">10 to 90%RH, No condensation</td></tr>
<tr><td rowspan="5">Vibration resistance</td><td rowspan="5">Conforming to JIS B 3502, IEC 61132-2</td><td rowspan="2">When there is intermittent vibration</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 57Hz</td><td>–</td><td>0.075mm</td><td rowspan="4">10 times each in X, Y and Z axis (80 minutes)</td></tr>
<tr><td>57 to 150Hz</td><td>9.8m/s^2</td><td>–</td></tr>
<tr><td rowspan="2">When there is continuous vibration</td><td>10 to 57Hz</td><td>–</td><td>0.035mm</td></tr>
<tr><td>57 to 150Hz</td><td>4.9m/s^2</td><td>–</td></tr>
<tr><td>Shock resistance</td><td colspan="6">Conforming to JIS B 3502, IEC 61131-2 (147m/s^2, 3 times each in 3 directions)</td></tr>
<tr><td>Operating environment</td><td colspan="6">No corrosive gas present</td></tr>
<tr><td>Operating height</td><td colspan="6">2000m (6562ft.) or less</td></tr>
<tr><td>Installation area</td><td colspan="6">On the control board</td></tr>
<tr><td>Over-voltage category*1</td><td colspan="6">II or less</td></tr>
<tr><td>Pollution degree *2</td><td colspan="6">2 or less</td></tr>
</table>

***1: Indicates the distribution area where the device is assumed to be connected, from the public power distribution network to the local machine device.**
Category II is applied to the devices to which the power is supplied from a fixed equipment.
The surge resistance voltage of a rated 300V device is 2500V.

***2: This is an index which indicates the occurrence rate of the conductive object in the environment where the device is used.**
Pollution degree 2 indicates that only non-conductive pollution may occur with a possibility of generating temporary conductivity due to accidental condensation.

***3: Do not use or install the PLC in the environment where higher atmospheric pressure is applied than at 0m elevation.**
Failure to observe this may result in malfunction.
Please consult your local Mitsubishi representative on use of PLC under increased pressure.

3.2 Performance Specifications

The following table gives the performance specifications of the A68ADN.

Table 3.2 Performance Specifications

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Analog input</td><td>Voltage: -10 to 0 to 10VDC (Input resistance: 1MΩ)
Current: -20 to 20mA (Input resistance: 250MΩ)
} Can be set with the input terminal</td></tr>
<tr><td>Digital output</td><td>Signed 16-bit binary (1/4000 setting : -4096 to 4095
1/8000 setting : -8192 to 8191
1/12000 setting : -12287 to 12287)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th rowspan="2">Analog Input</th><th colspan="3">Digital output value (gain: 5V/20mA, offset: 0V/0mA)</th></tr>
<tr><th>1/4000 setting</th><th>1/8000 setting</th><th>1/12000 setting</th></tr>
<tr><td>10V</td><td>+4000</td><td>+8000</td><td>+12000</td></tr>
<tr><td>5V or 20mA</td><td>+2000</td><td>+4000</td><td>+6000</td></tr>
<tr><td>0V or 0mA</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>-5V or -20mA</td><td>-2000</td><td>-4000</td><td>-6000</td></tr>
<tr><td>-10V</td><td>-4000</td><td>-8000</td><td>-12000</td></tr>
</table>
(Factory setting: gain ... 5V, offset ... 0V)</td></tr>
<tr><td>Maximum resolution</td><td>
<table>
<tr><th></th><th>1/4000 setting</th><th>1/8000 setting</th><th>1/12000 setting</th></tr>
<tr><td>Voltage input</td><td>2.5mV</td><td>1.25mV</td><td>0.83mV</td></tr>
<tr><td>Current input</td><td>10 μA</td><td>5 μA</td><td>3.33 μA</td></tr>
</table></td></tr>
<tr><td>Overall accuracy*</td><td>
<table>
<tr><th></th><th>1/4000 setting</th><th>1/8000 setting</th><th>1/12000 setting</th></tr>
<tr><td>±1%</td><td>±40</td><td>±80</td><td>±120</td></tr>
</table></td></tr>
<tr><td>Maximum conversion speed</td><td>20msec/1 channel</td></tr>
<tr><td>Absolute maximum input</td><td>Voltage: ±15V Current: ±30mA</td></tr>
<tr><td>Number of analog input device point</td><td>8 channels/1 module</td></tr>
<tr><td>Isolation specifications</td><td>
<table>
<tr><th>Specific isolated area</th><th>Isolation method</th><th>Dielectric withstand voltage</th><th>Insulation resistance</th></tr>
<tr><td>Between I/O terminal and PLC power supply</td><td>Photocoupler isolation</td><td>500V AC for 1 minute</td><td>5M Ω or more (measured with a 500V DC insulation resistance tester)</td></tr>
<tr><td>Between channels</td><td>Not isolated</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>Number of occupied I/O points</td><td>32 device points (special)</td></tr>
<tr><td>Connection terminal</td><td>38-device point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2mm^2 (Applicable tightening torque: 39 to 59N-cm)</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>Internal current consumption(5V DC)</td><td>0.4A</td></tr>
<tr><td>Weight kg (lb)</td><td>0.51kg (1.13lb)</td></tr>
<tr><td>External dimensions mm (in)</td><td>250 (9.84) (H) × 37.5 (1.48) (W) × 131 (5.16) (D)</td></tr>
</table>

*** This is the accuracy to the maximum digital output value. The maximum digital output value is the maximum value of the selected resolution. The value is the same for the current input and voltage input.**

POINT

Analog input allowed for maximum resolution and overall accuracy is from –10 to 0 to 10V or from –20 to 0 to 20mA.

3.3 I/O Conversion Characteristics

Input/output (hereafter I/O) conversion characteristics are expressed by the angle of the line connecting the offset value and gain value used to convert the analog signals (voltage or current input) from outside of the PLC, into digital values. This is shown in Figure 3.1 below.

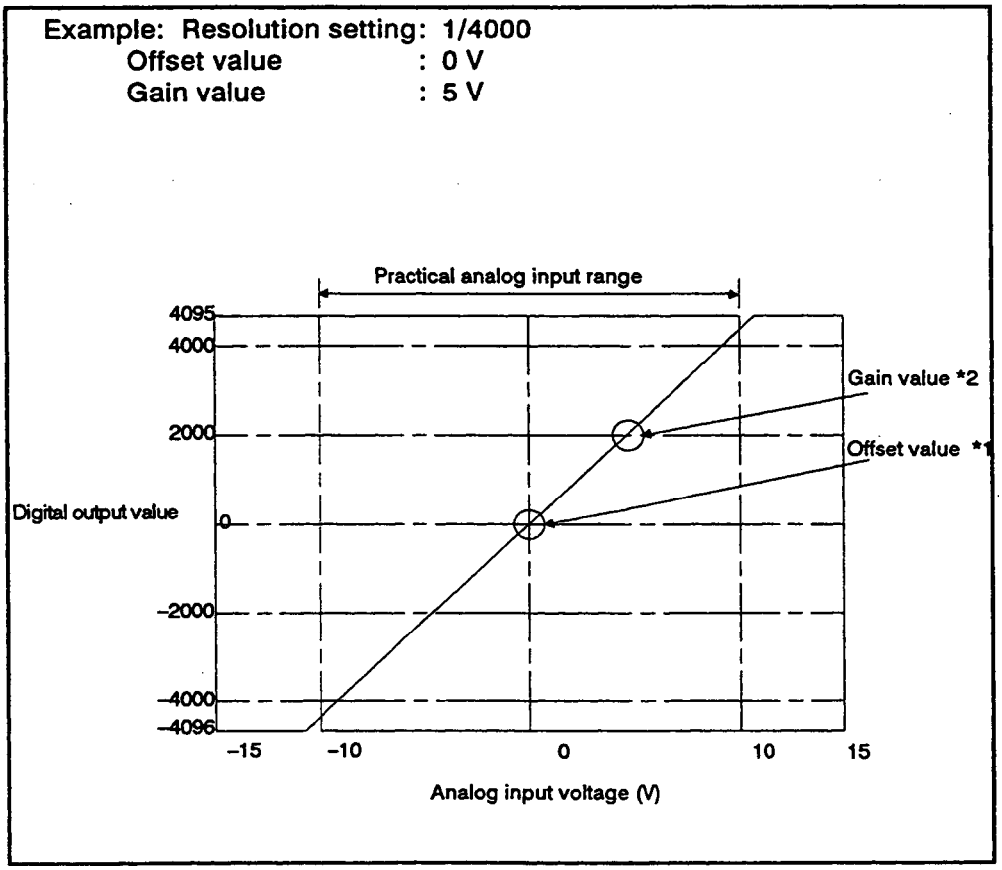


Fig.3.1 I/O Conversion Characteristics

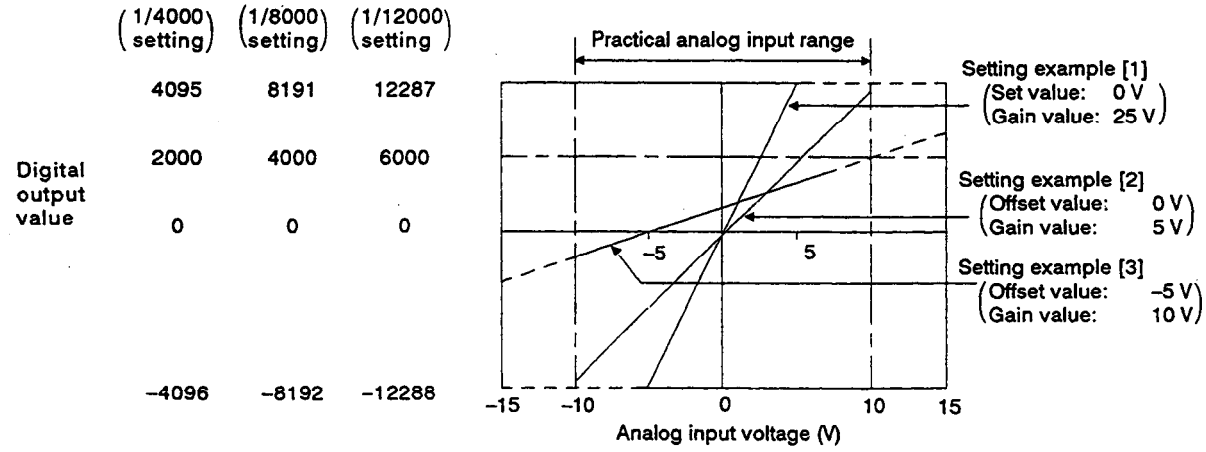
*1 Analog input value (voltage or current) corresponding to the digital output value of "0"

*2 Analog input value (voltage or current) corresponding to the following digital output values:

2000 with resolution setting of 1/4000
4000 with resolution setting of 1/8000
6000 with resolution setting of 1/12000

3.3.1 Voltage input characteristics

Figure 3.2 shows the voltage input characteristics for three different offset/gain combinations.



Setting Example No.	Offset Value	Gain value	Digital Output Value with +3 V Analog Input			Digital Output Value with -3 V Analog Input		
			1/4000 Setting	1/8000 Setting	1/12000 Setting	1/4000 Setting	1/8000 Setting	1/12000 Setting
1	0V	2.5V	2400	4800	7200	-2400	-4800	-7200
2	0V	5V	1200	2400	3600	-1200	-2400	-3600
3	-5V	10V	1066	2132	3198	266	532	798

Figure 3.2 Voltage Input Characteristics

POINT

(1) If the input voltage is in the range of -10 to 0 to 10V, the maximum resolution and overall accuracy are within the range of performance specifications. However, if the input voltage exceeds this range, resolution and accuracy may be out of the specified range. (The values on the dotted lines should not be used, since they may not meet the accuracy.)

(2) Inputting an analog voltage that causes the digital output value to exceed the maximum value (4095/8191/12287) or to become smaller than the minimum value (-4096/-8192/-12288), fixes the result of the A-D conversion (digital output value) at either the maximum value (4095/8191/12287) or the minimum value (-4096/-8192/-12288).

(3) Do not apply ±15V or more. This may damage the module.

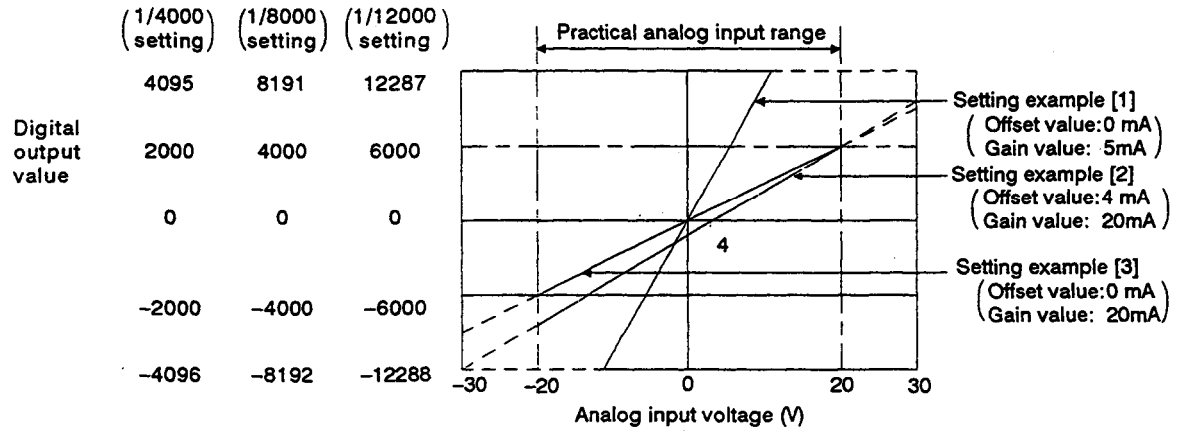
(4) When setting the gain or offset, the following must be satisfied:

(Gain value) - (Offset value) ≧ 1 V (1/4000 setting)/1.5 V (1/8000 setting)/2 V (1/12000 setting)

If the set values do not satisfy the relationship stated above, the obtained digital output values will not be correct.

3.3.2 Current input characteristics

Figure 3.3 shows the voltage input characteristics for three different offset/gain combinations.



Setting Example No.	Offset Value	Gain value	Digital Output Value with +7 mA Analog Input			Digital Output Value with -3 mA Analog Input		
			1/4000 Setting	1/8000 Setting	1/12000 Setting	1/4000 Setting	1/8000 Setting	1/12000 Setting
1	0mA	5mA	2800	5600	8400	-1200	-2400	-3600
2	4mA	20mA	375	750	1125	-875	-1750	-2625
3	0mA	20mA	700	1400	2100	-300	-600	-900

Figure 3.3 Current Input Characteristics

POINT

(1) When the input voltage is in the range from -20 to 0 to +20mA, the maximum resolution and overall accuracy are within the range of performance specifications. However, if input current exceeds this range, resolution and accuracy may be out of the specified range. (The values on the dotted lines should not be used, since they may not meet the accuracy.)

(2) Inputting an analog current that causes the digital output value to exceed the maximum value (4095/8191/12287) or to become smaller than the minimum value (-4096/-8192/-12288), fixes the result of the A-D conversion (digital output value) at either the maximum value (4095/8191/12287) or the minimum value (-4096/-8192/-12288).

(3) Do not apply ±30mA or more. This may damage the module.

(4) When setting the gain or offset, the following must be satisfied:

(Gain value) - (Offset value) ≧ 4 mA (1/4000 setting)/6 mA (1/8000 setting)/8 mA (1/12000 setting)

If the set values do not satisfy the relationship stated above, the obtained digital output values will not be correct.

3.3.3 Relationship between the offset/gain setting and the digital output values

(1) Resolution

Resolution is obtained using the following expression:

● Voltage input

$$\text{Resolution} = \frac{\text{(Gain value) - (Offset value)}}{\text{2000 (for 1/4000 setting)/4000 (for 1/8000 setting)/6000 (for 1/12000 setting)}} \times 1000\ (\text{mV})$$

● Current input

$$\text{Resolution} = \frac{\text{(Gain value) - (Offset value)}}{\text{2000 (for 1/4000 setting)/4000 (for 1/8000 setting)/6000 (for 1/12000 setting)}} \times 1000\ (\mu\text{A})$$

(2) Relationship between the maximum resolution and the digital output value

If the setting of offset/gain values causes the following, the digital value does not change in increments of "1".

$$\frac{\text{(Gain value) - (Offset value)}}{\text{2000/4000/8000}} < \text{(Maximum resolution)}$$

Figures 3.4 to 3.7 show the relationship between the offset/gain settings and the digital output values.
The offset and gain values in these figures are those in the voltage and current input characteristics figures in Sections 3.3.1 and 3.3.2.

(3) Overall accuracy

The overall accuracy is the accuracy to the maximum digital output value.
Even if the input characteristics are changed by changing the offset/gain setting, the overall accuracy will not change and will be kept within the range of the performance specifications. The overall accuracies of the voltage/current input characteristics are shown in Fig. 3.4 and Fig. 3.5.

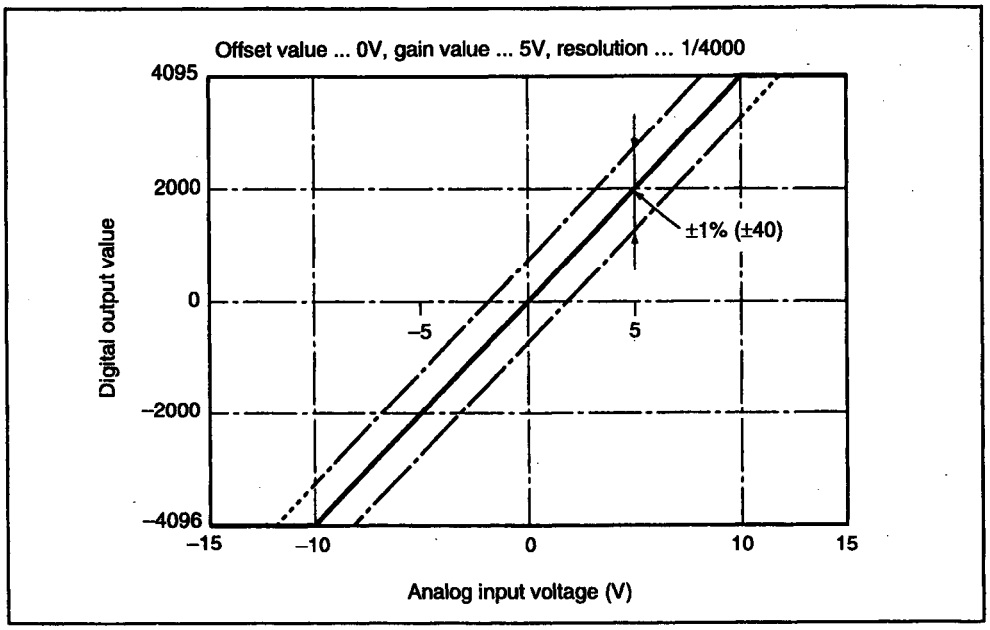


Fig. 3.4 Overall accuracy of voltage input characteristics

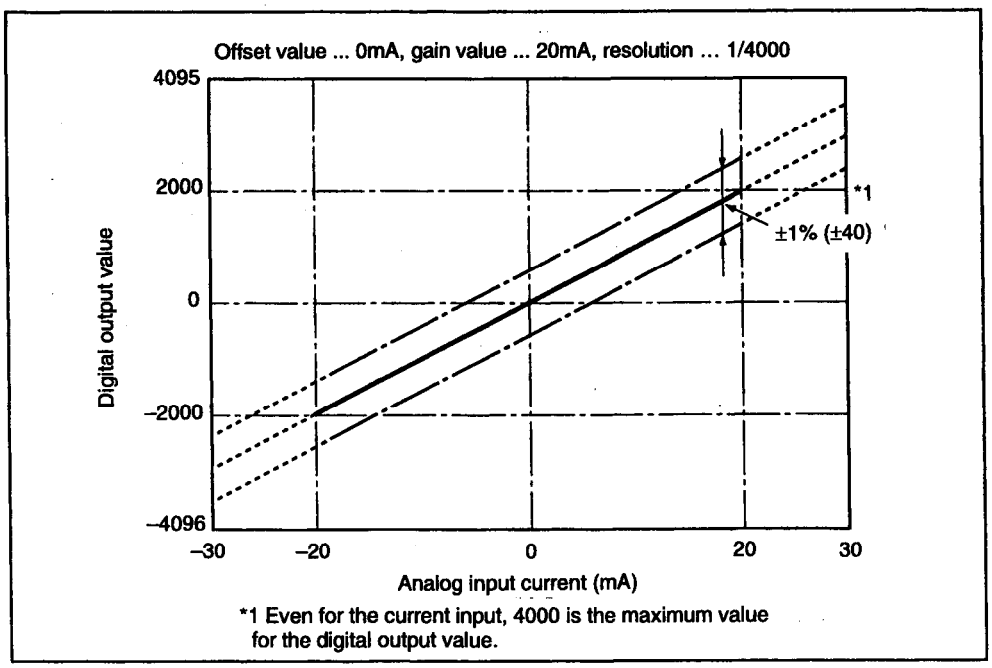
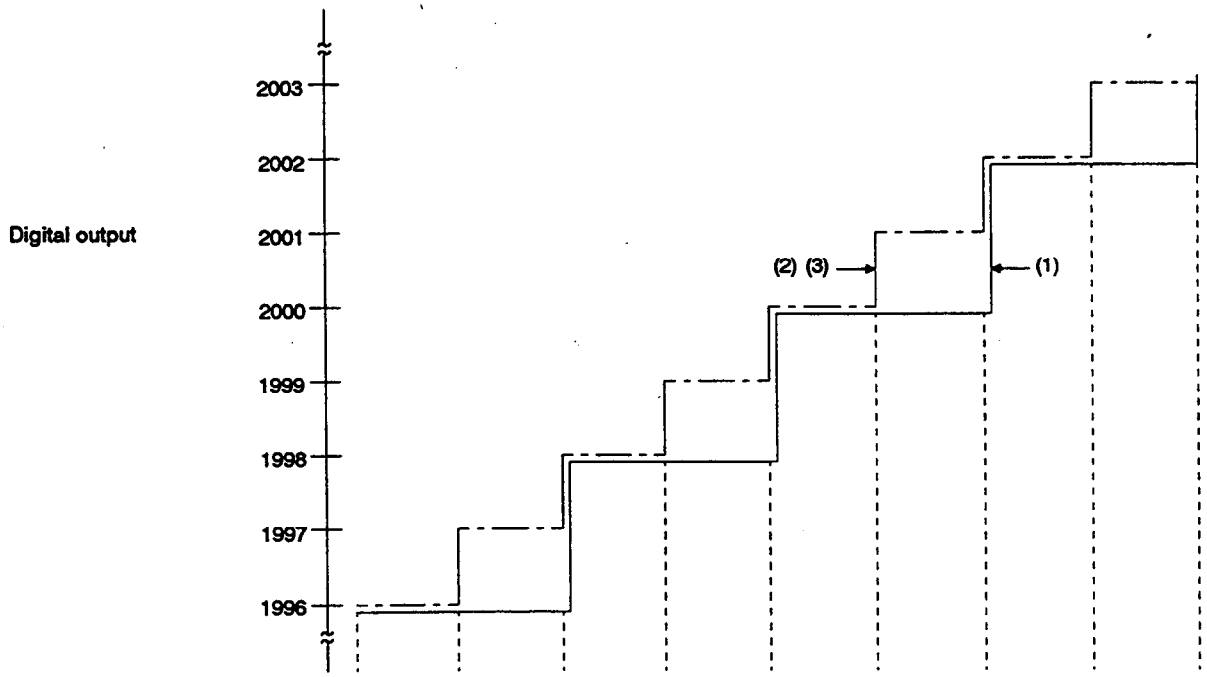


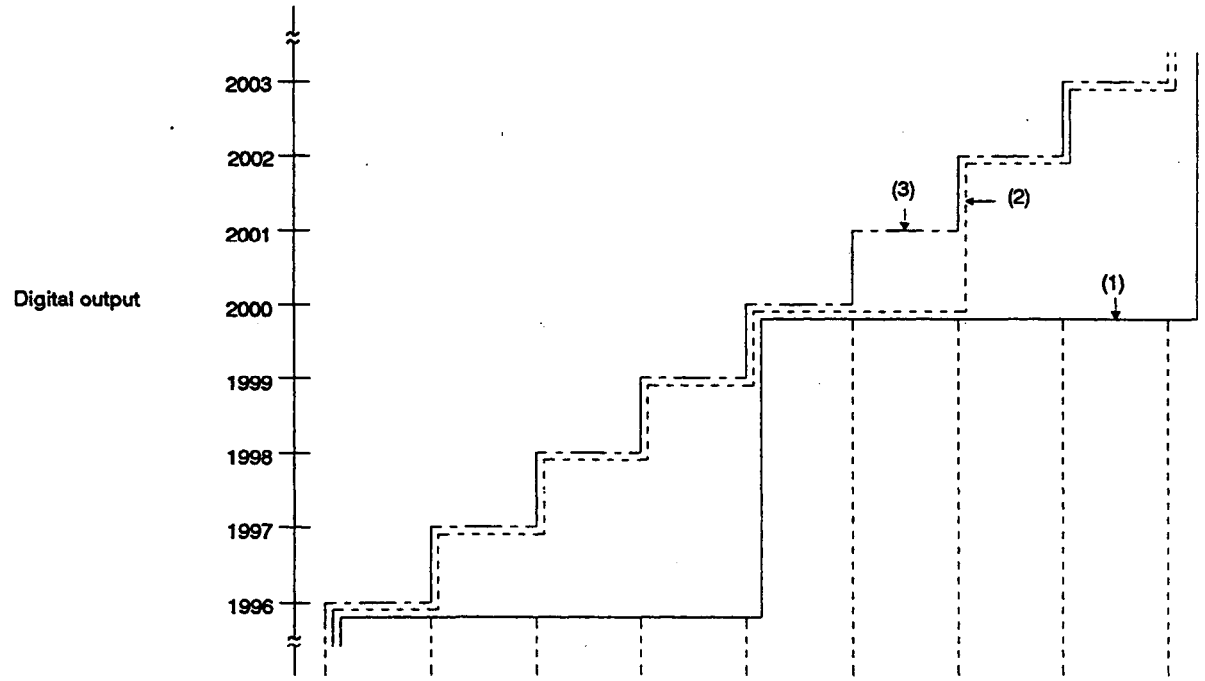
Fig. 3.5 Overall accuracy of current input characteristics



No.	Offset Value	Gain Value	Reso-lution	Analog Input Value (V)							
1	0 V	2.5 V	1/4000	2.4950 to 2.4975		2.4975 to 2.5000		2.5000 to 2.5025		2.5025 to 2.5050	
			1/8000	1.2475 to 1.2488		1.2488 to 1.2500		1.2500 to 1.2513		1.2513 to 1.2525	
			1/12000	0.8317 to 0.8325		0.8325 to 0.8334		0.8334 to 0.8342		0.8342 to 0.8350	
2	0 V	5 V	1/4000	4.9900 to 4.9925	4.9925 to 4.9950	4.9950 to 4.9975	4.9975 to 5.0000	5.0000 to 5.0025	5.0025 to 5.0050	5.0050 to 5.0075	5.0075 to 5.0100
			1/8000	2.4950 to 2.4936	2.4936 to 2.4975	2.4975 to 2.4988	2.4988 to 2.5000	2.5000 to 2.5013	2.5013 to 2.5025	2.5025 to 2.5038	2.5038 to 2.5050
			1/12000	1.6634 to 1.6642	1.6642 to 1.6650	1.6650 to 1.6659	1.6659 to 1.6667	1.6667 to 1.6675	1.6675 to 1.6684	1.6684 to 1.6692	1.6692 to 1.6700
3	−5 V	10 V	1/4000	9.9700 to 9.9755	9.9755 to 9.9850	9.9980 to 9.9925	9.9925 to 10.0000	10.0000 to 10.0075	10.0075 to 10.0150	10.0150 to 10.0225	10.0225 to 10.0300
			1/8000	4.9850 to 4.98888	4.9888 to 4.9925	4.9925 to 4.9963	4.9963 to 5.0000	5.0000 to 5.0038	5.0038 to 5.0075	5.0075 to 5.0113	5.0113 to 5.0150
			1/12000	3.3234 to 3.3259	3.3259 to 3.3284	3.3284 to 3.3309	3.3334 to 3.3359	3.3359 to 3.3384	3.3359 to 3.3384	3.3384 to 3.3409	3.3409 to 3.3434

*** With the gain and offset setting as in No.1, the digital output values will not increase/decrease by one, since the analog input values exceed the maximum resolution (in section 3.2).**

Figure 3.6 Voltage Input and Digital Output Values



No.	Offset Value	Gain Value	Reso-lution	Analog Input Value (mA)						
1	0 mA	5 mA	1/4000	4.9900 to 5.0000				5.0000 to 5.0100		
			1/8000	2.4950 to 2.5000				2.5000 to 2.5050		
			1/12000	1.6634 to 1.6667				1.6667 to 1.6700		
2	4 mA	20 mA	1/4000	19.9680 to 19.9760	19.9970 to 19.9840	19.9840 to 19.9920	19.9920 to 20.0000	20.0000 to 20.0160	20.0160 to 20.0240	20.0240 to 20.0320
			1/8000	9.9840 to 9.9880	9.9980 to 9.9920	9.9920 to 9.9960	9.9960 to 1.0000	10.0000 to 10.0080	10.0080 to 10.0120	10.0120 to 10.0160
			1/12000	6.6560 to 6.6587	6.6587 to 6.6614	6.6614 to 6.6640	6.6640 to 6.6667	6.6667 to 6.6720	6.6720 to 6.6747	6.6747 to 6.6774

*** With the gain and offset settings as in No.1 and No.2, the digital output values will not increase/decrease by one, since the analog input values exceed the maximum resolution (in section 3.2).**

Figure 3.7 Current Input and Digital Output Values

3.4 Functions

Table 3.3 A68and Functions

Item	Descriptions	Section Ref.
A-D conversion enable/disable setting	● Enable/disable setting is available for each channel. (Default: Enable for all channels) ● Sampling time can be shortened by setting "disable" for the unused channels.	3.7.1
Offset/gain setting	● Offset/gain setting is available for each channel without a volume dial to change I/O conversion characteristics.	3.3
Averaging processing specification	● By specifying the number of frequencies or time duration for each channel, A-D conversion data is averaged and the result is set to buffer memory as the digital output value.	3.7.2

3.5 Maximum Conversion Speed

Conversion speed is the period of time from channel switching to the writing the digital value to buffer memory.

3.5.1 Conversion speed per channel

Conversion speed per channel is 20 msec.

If more than one channel is used, the sampling time will be "(20 msec) x (number of conversion-enabled channels)".

3.5.2 Influence of [FROM]/[TO] instruction executions on maximum conversion speed.

The maximum conversion speed indicated in 3.5.1 assumes that the [FROM]/[TO] instruction is not executed. If the [FROM]/[TO] instruction is executed:

(1) Digital value write to the buffer memory is suspended during [FROM]/[TO] processing until the [FROM]/[TO] processing is completed.

(2) Channel switching is suspended during [FROM]/[TO] processing until [FROM]/[TO] processing is completed.

(3) [FROM]/[TO] processing is suspended during digital value write to the buffer memory or channel switching until the write or channel switching process is completed.

(4) The [FROM]/[TO] instruction should be specified to transfer more than one data simultaneously. Processing is less influenced if the number of [FROM]/[TO] instructions is smaller.

3.6 I/O List for PC CPU

The A68ADN uses 32 input and 32 output device points for data communications with the PC CPU. I/O signal assignment and functions are shown in Table 5.1.

Device X indicates an input signal from the A68ADN to the PC CPU and device Y an output signal from the PC CPU to the A68ADN. I/O numbers (X, Y) and I/O addresses used in this manual assume that the A68ADN is mounted as slot 0 of the main base unit.

Table 3.4 I/O Signals

Signal Direction (A68ADN to PC CPU)		Signal Direction (PC CPU to A68ADN)	
Device No.	Signal Name	Device No.	Signal Name
X0	Watchdog timer error (Detected by A68ADN)	Y0 to YC	N/A
X1	A – D conversion ready		
X2	Error flag		
X3 to X1C	N/A	YD to YF	[RFRP] [RTOP] instruction interlock signals Only used when the A68ADN is used in a remote I/O station
		Y10 Y11	N/A
		Y12	Error reset
X1D to X1F	[RFRP] [RTOP] instruction interlock signals Only employed when the A68ADN is used in a remote I/O station	Y13 to Y1F	N/A

POINT

If output Y0 to YC, Y10 to Y11, and Y13 to Y1F should be turned ON/OFF in the sequence program, the A68ADN functions would not be guaranteed. Y0 to Y1F (corresponding to X0 to X1F) cannot be used as internal relays.

(1) Watchdog timer error (X0)

The X0 signal goes ON when the A68ADN (using the self-diagnosis function) detects a watchdog timer error.

When a watchdog timer error occurs, the A68ADN stops A-D conversion.

If the X0 signal turns ON, it indicates that the A68ADN hardware is faulty.

(2) A – D conversion ready (X1)

The X1 signal goes ON when A-D conversion processing is ready in a normal (other than test) mode when the power supply to the PC CPU goes ON or the PC CPU is reset.

The signal goes OFF when the test terminals on the front panel are shorted.

This signal can be used as an interlock for buffer memory read/write operations.

REMARK

Definition of A-D conversion-ready status: When A-D conversion is completed in all eight channels and the digital output values are stored in buffer memory.

IMPORTANT

A FROM/TO instruction cannot be executed in the test mode. Use the D/A conversion ready signal (X1) as an interlock for any program that contains a FROM/TO instruction.

If a FROM/TO instruction is executed in the test mode, the preset offset and/or gain value might be lost, or a CPU error may occur causing the calculation to stop.

(3) Error flag (X2)

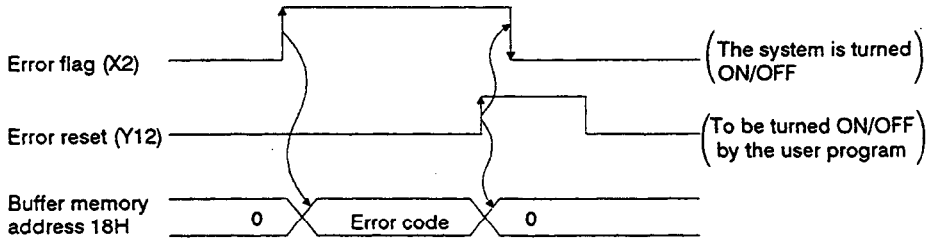
The X2 signal goes ON when an error (other than a watchdog timer error) is detected by the A68ADN. When the X2 signal is turned ON, an error code is stored in the error code storage area in buffer memory.

The signal goes OFF when the error reset signal (Y12) is turned ON.

(4) Error reset (Y12)

Turning Y12 ON causes the error flag (X2) to go OFF and writes "0" to the error code storing area (address 18H) in buffer memory, after clearing the error code stored there.

The RUN LED, which flashes on the front panel after an error is detected, stops flashing when the Y12 signal is turned ON (which indicates "normal operation").



3.7 Buffer Memory

The A68ADN uses the buffer memory (not battery-backed) for data communications with a PC CPU.

Buffer memory allocations are shown below.

Address (decimal)		Default value	
0	A-D conversion-enabled/disabled setting	00FFH (all channels enabled)	..... See Section 3.7.1
1	Averaging processing specification	0 (sampling processing for all channels)	..... See Section 3.7.2
2	CH1 averaging time, count	0	
3	CH2 averaging time, count		
4	CH3 averaging time, count		
5	CH4 averaging time, count		
6	CH5 averaging time, count		
7	CH6 averaging time, count		
8	CH7 averaging time, count		
9	CH8 averaging time, count		
10	CH1 digital output value	0	
11	CH2 digital output value		
12	CH3 digital output value		
13	CH4 digital output value		
14	CH5 digital output value		..... See Section 3.7.3
15	CH6 digital output value		
16	CH7 digital output value		
17	CH8 digital output value		
18	Write data error code	0 (no error)	..... See Section 3.7.4
19	A-D conversion-completion flag	00FFH (A-D conversion completed for all channels)	..... See Section 3.7.5
20	Resolution setting	1 (1/4000)	..... See Section 3.7.6

POINT

Buffer memory addresses 10 to 17 are reserved for read only. If data is written to them using a sequence program, the RUN LED begins flashing and an error code is stored in buffer memory address 18.

3.7.1 A-D conversion-enabled/disabled setting

Whether A-D conversion is to be executed or not is written to buffer memory address 0 for each channel ("1" for enable and "0" for disable).

The sampling cycle can be shortened by setting "disable" for the unused channels. The default value for each channel is set as an A-D conversion.

Examples:

(1) Sampling cycle time when "enable" is set for all channels:

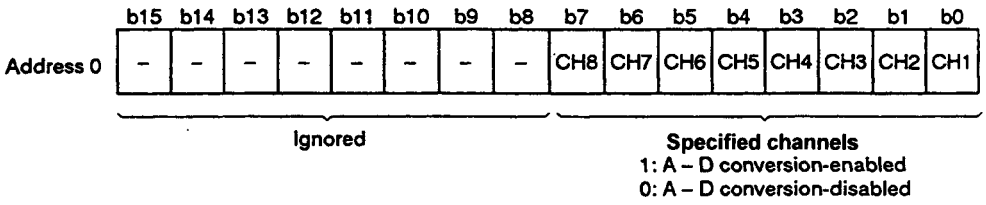
8 (number of enabled channels) x 20 msec (conversion speed per channel) = 160 msec

(2) Sampling cycle time when "enable" is set for channels 1 and 3:

2 (number of enabled channels) x 20 msec (conversion speed per channel) = 40 msec

(1) Enable/disable setting method

Enable or disable is set for each channel.



(2) Process of the A68ADN for enable/disable setting

(a) Initialization for averaging processing

For averaging processing, the data stored in the work area by the A68ADN system software is initialized.

The digital values in buffer memory keep the data prior to the setting of enable/disable.

If conversion-enabled/disabled setting is made when the A68ADN completes 30 counts of sampling process at a channel for which 50 counts of averaging process, the sampling data collected during the sampling period will be cleared and averaging processing will be executed from the beginning

(b) Resetting the A-D conversion-completion flag

The A-D conversion-completion flag (address 19 in buffer memory) for channels 1 to 8 is reset.

3.7.2 Setting for sampling processing/averaging processing

(1) Digital value output in sampling processing and averaging processing

(a) Sampling processing

The analog values input to the channels are converted 1:1 to digital output values. These digital output values are then stored in buffer memory.

(b) Averaging processing

The A68ADN does the A-D conversion as often as specified count or during the specified time for the channel which is specified by the PC CPU for averaging processing. An average is calculated (excluding the minimum and maximum values) and stored in buffer memory. If the specified count of processings is two or less, sampling processing is executed instead of averaging processing.

When A-D conversion-enabled/disabled setting is made, data stored in the work area is initialized.

POINT

(1) **When sampling processing is specified:**

As the A68ADN's PC CPU scans each channel, the value appearing at that instant is written to the buffer memory as a digital value. The timing of this sampling depends on the number of A-D conversion-enabled channels, and may be found by using the following formula:

(processing time) =
(number of A – D conversion – enabled channels) x 20 (msec/1 channel)
↑ Maximum conversion speed

Example: When conversion-enabled is set for channels 1, 2, 3, 5, and 6:
Processing time = 5 x 20 = 100 (msec)

(2) Averaging processing by specifying time

(a) **Averaging processing is specified in 10 msec units. Values less than 10 msec are rounded down.**

Example: If 1234 msec is set, it is processed as 1230 msec.

(b) **The count of processing within the set time varies with the number of A-D conversion-enabled channels.**

$$\text{Processing count} = \frac{\text{Time setting}}{\text{(number of A – D conversion-enabled channels)} \times 20\ \text{(msec/channel)}}$$

Maximum conversion speed ↑

Example: Number of A-D conversion-enabled channels = 4, Time setting = 8000 msec
8000 ÷ (4 x 20) = 100 times

(3) Averaging processing by specifying a number of counts

The time in which the average value by this processing is stored in the buffer memory varies with the number of A-D conversion-enabled channels.

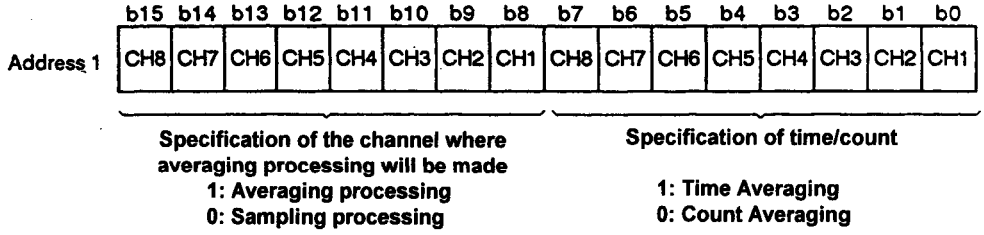
Processing time = (count setting) x (A-D conversion-enabled channels) x 20 (msec/channel)
↑ Maximum conversion speed

Example: When A-D conversion-enabled is set for channels 1, 2, 3 and 4, Count setting = 50
50×4×20=4000(msec)

(2) **Specification of averaging Processing and selection of time averaging or count averaging**

(a) When the power is turned ON and the A68ADN A-D conversion-ready signal is ON, all channels are set for sampling processing.

(b) For selection of sampling processing or averaging processing, use address 1 of the buffer memory.



POINT

(1) For averaging processing, "count" or "time" must be set in advance.

(2) When averaging processing is not specified, sampling processing is set without regard to the specification of time/count.

(3) Setting "time" or "count"

(a) For the channels specified for averaging processing, write the "time" or "count" to the buffer memory addresses (2 to 9) corresponding to those channels.

When the power is turned ON, the setting for "time" and "count" is "0".

(b) The setting ranges are as indicated below:

"Count" averaging processing: 1 to 500 counts

"Time" averaging processing: 160 to 1000 msec

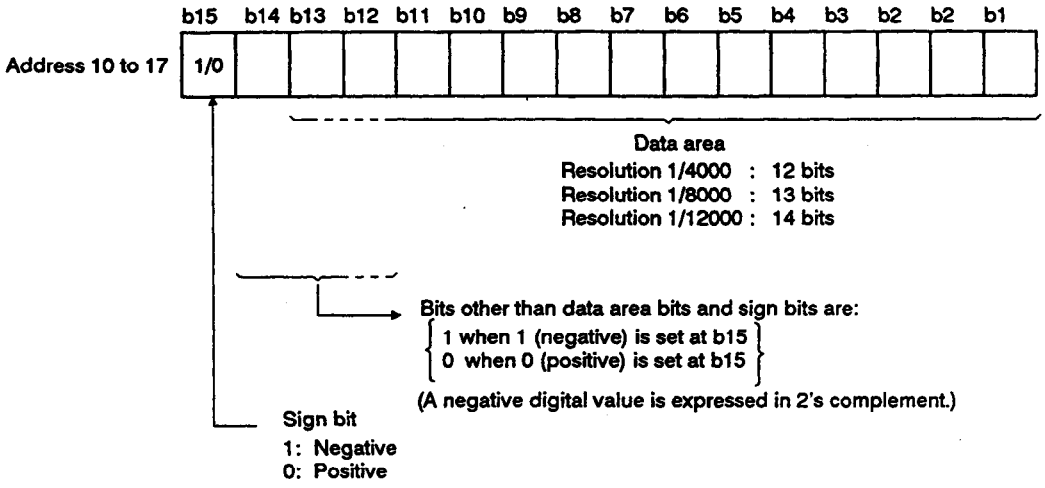
POINT

If a value outside the above ranges is written, a setting error occurs and the set value in buffer memory does not change. However, the A68ADN performs A – D conversion processing based on the averaging time or count previously set.

3.7.3 Digital output values

Digital values converted from analog are stored to buffer memory addresses 10 to 17 for each channel.

Digital output values are 16-bits, singed binary. The ranges vary depending on the resolution setting, as indicated below:



3.7.4 Write data error code

(1) **When data is written to the A68ADN from the PC CPU, the A68ADN checks the data range and read/write area access only once. If the written data is outside the specified range, an error code is stored (as a 16-bit binary value) in buffer memory address 18.**

See Section 6.1 for error code details.

(2) **If more than one type of error occurs, only the error code of the first error is stored in the A68ADN.**

(3) **To reset the error code, use the sequence program to turn Y12 ON (see Section 5.1).**

(4) **When an error is reset, the data error code is set to 0 and the RUN LED of the A68ADN stops flashing to be on.**

3.7.5 A-D conversion-completion flag

(1) When the power is turned ON, the A – D conversion-ready signal (X1) goes ON. This indicates that the A – D conversion-completion flag is ready for all channels from 1 to 8. OOFFH is stored in buffer memory.

(2) **After the power is turned ON, A/D conversion-completion flag is processed only once if the setting for A-D conversion-enable/disabled at address 0 is changed.**

- A – D conversion-disabled → enabled:

  When averaging processing is specified, averaging processing is executed a preset number of counts or for a preset length of time. After the processing is completed, the digital value (obtained after A-D conversion) is then stored in buffer memory. The flag is then set to 1.

- A – D conversion-enabled → disabled:

  The relevant channel's A – D conversion-completion flag is set to 0.

(3) Each channel has an A-D conversion-completion flag.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Address 0	0	0	0	0	0	0	0	0	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

A – D conversion-completion flag
1: A – D conversion completed
0: A – D conversion not completed

(4) **The A/D conversion-completion flag can be used for the interlock when reading the digital value of the channel for which averaging processing will be executed.**

3.7.6 Setting resolution

(1) Set the digital output value resolution to "1/4000", "1/8000", or "1/12000".
When the power is turned ON, the default is set at 1/4000

(2) **Write a number (1 to 3) to address 20 for resolution setting.**

Setting	Resolution
1	1/4000
2	1/8000
3	1/12000

POINT

Set the resolution only once while the PC CPU is running and before the A-D conversion-enabled/disabled setting is made.

If the setting is changed while the A-D conversion is set for enabled, the correct digital output values will not be obtained.

MEMO

4. PRE-OPERATION SETTINGS AND PROCEDURES

4.1 Handling Instructions

(1) Do not drop the module or subject it to strong impact, since the case and terminal adapter are made of resin.

(2) Do not remove the printed circuit board from the case.
Failure to observe this instruction may result in breakdown.

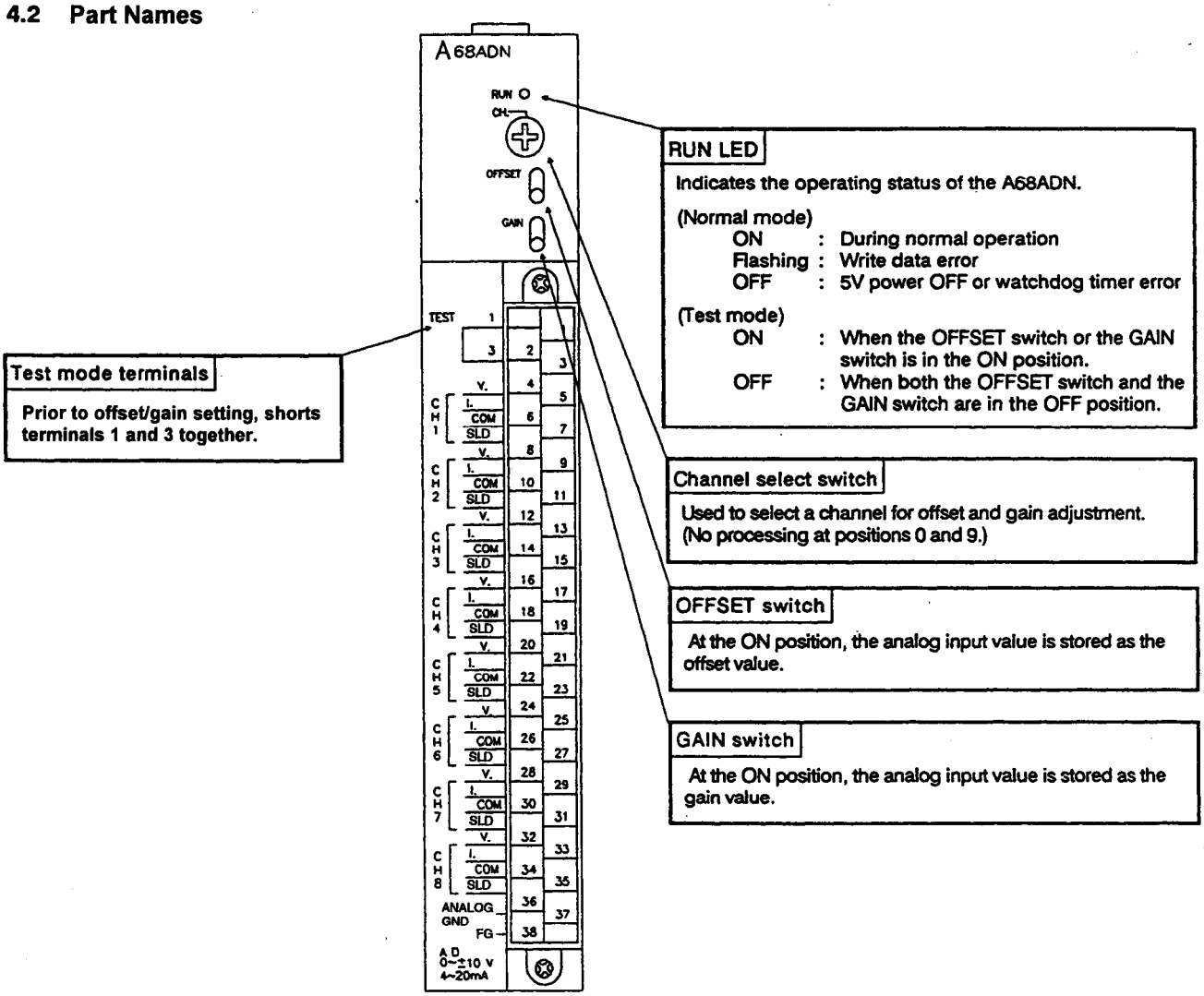
(3) Be careful not to get the foreign matters such as wire off cuts inside the module from its upper part during wiring. If they get inside the module, please remove them.

(4) Tighten terminal screws within the following range.

Screw	Tightening Torque Range
I/O terminial block terminal screws (M3)	39 to 59 N·cm
I/O terminal block installation screws (M4)	78 to 118 N·cm

(5) To mount the module onto the base, press the module against the base so that the hook is securely locked. To remove the module, push the catch on top of the module, and, after the hook is disengaged from the base, pull the module toward you.

4.2 Part Names



Switches marked with ☐ are valid only in the test mode. See Section 4.3 for details.

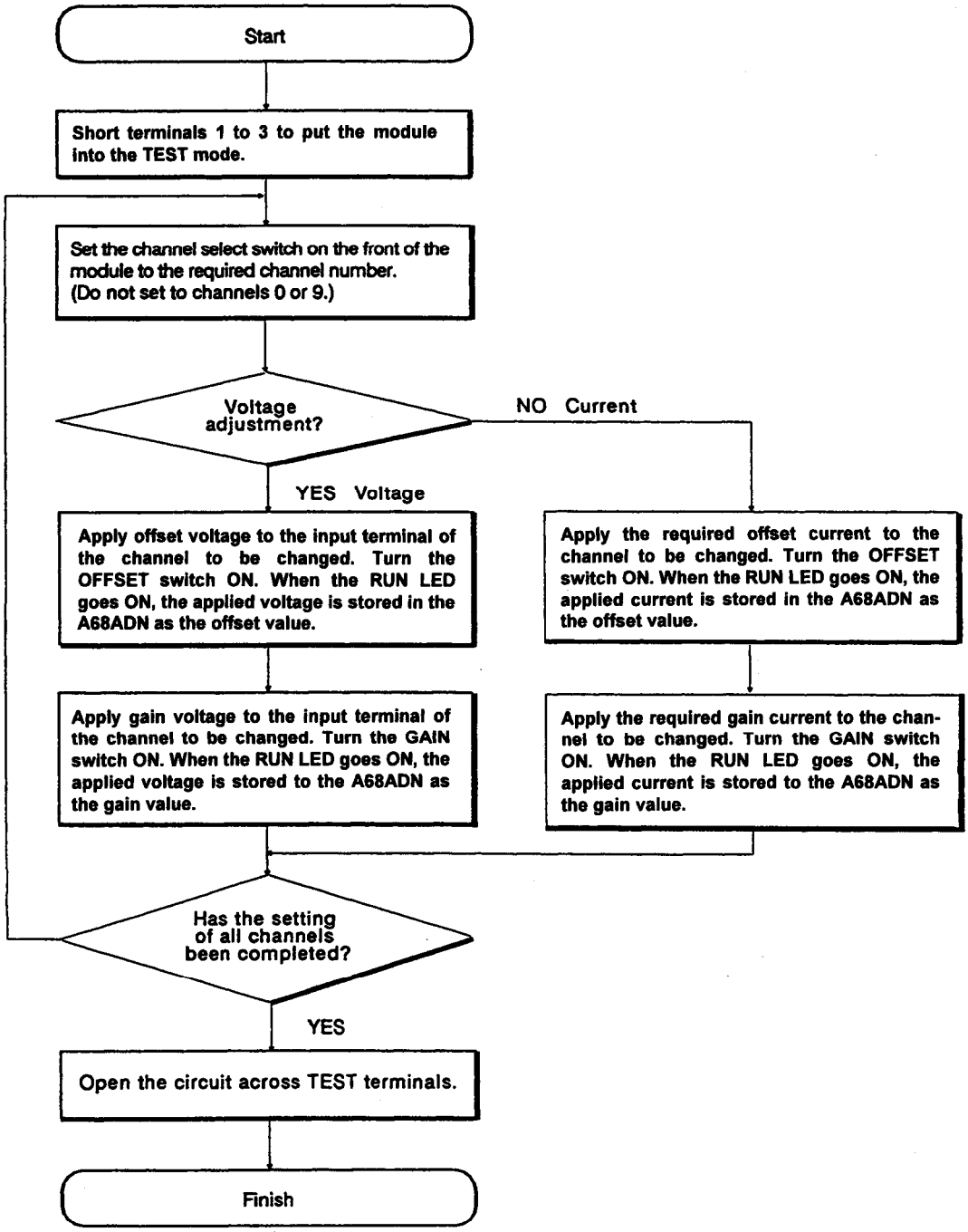
Terminal No.	Signal Name		Terminal No.	Signal Name		Terminal No.	Signal Name	
1	TEST		13	CH3	V+	25	CH6	V+
2	Open		14		I+	26		I+
3	TEST		15		COM	27		COM
4	Open		16		SLD	28		SLD
5	CH1	V+	17	CH4	V+	29	CH7	V+
6		I+	18		I+	30		I+
7		COM	19		COM	31		COM
8		SLD	20		SLD	32		SLD
9	CH2	V+	21	CH5	V+	33	CH8	V+
10		I+	22		I+	34		I+
11		COM	23		COM	35		COM
12		SLD	24		SLD	36		SLD
						37	ANALOG GND	
						38	FG	

4.3 Offset/Gain Settings

Change the I/O characteristics according to the following chart.

The factory settings are:

Voltage input ..... Offset value : 0 V
Gain value : 5 V
Current input ..... Offset value : 0 mA
Gain value : 20 mA



POINT

(1) Set the offset and gain values under conditions of actual use.

(2) The offset and gain values are stored in the A68ADN and are not erased if the power is turned OFF.

(3) Set the offset/gain values with the PC CPU in the stop mode. If the module is set to the test mode, A-D conversion is stopped on all channels.
Therefore, use the A-D conversion ready signal as an interlock.

(4) Set the offset/gain values within the range of -10 to 0 to 10 VDC or -20 to 0 to 20 mA. If set outside these ranges, maximum resolution and overall accuracy may not be within the specified ranges.

(5) If grounding at the point marked with *5 described in Section 4.4.2 (no ground--ground, or ground--removal), redo offset/gain setting from the first step.

4.4 Wiring

4.4.1 Wiring instructions

Take the following precautions to protect external wiring from noise:

(1) **Separate the AC wiring from the A68ADN external input signal wiring.**

(2) Separate the main circuit and/or high voltage wiring from the control and signal wiring.

(3) When applicable, ground the shielding of all wires to a common ground point.

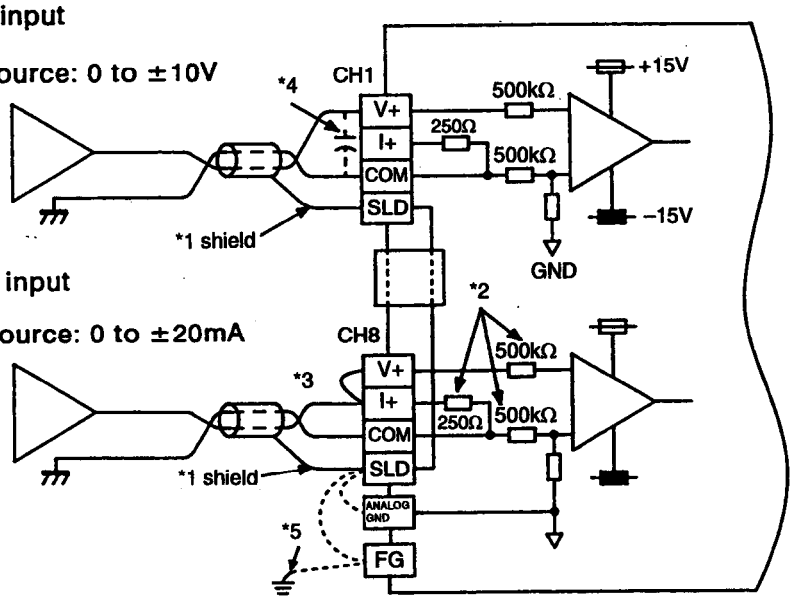
4.4.2 Module connection example

(1) Voltage input

Signal source: 0 to ±10V

(2) Current input

Signal source: 0 to ±20mA



*1: For the cable, use a two-core twisted shielded wire.

*2: Indicates the input resistance of the A68ADN.

*3: For current input, make sure to connect the terminals (V+) and (I+).

*4: **If noise or ripple is generated at the external wiring, connect a capacitor (approximate 0.1 to 0.47μF, 25V or more withstand voltage) between terminals V and COM.**

*5: If there is excessive noise, ground the module. If any change has been made in grounding method (ground/no ground) after offset/gain setting, redo the setting.

4.5 Inspection and Maintenance

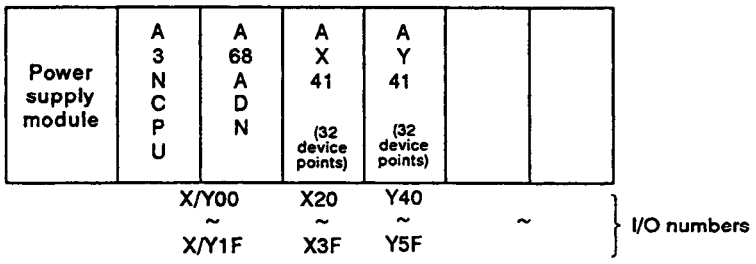
The A68ADN module does not require special inspections after installation. However, to ensure that the system operates at its best, the module should be checked following the instructions in the User's Manual for the particular PC CPU.

MEMO

5. PROGRAMMING

5.1 Initial setting program and digital output value read program

[Conditions]



(1) System configuration

(2) Initial setting

(a) A-D conversion-enabled channels ..... Channels 1, 2, 3, and 5

(b) Averaging processing by count.....Channel 3 (setting: 50 times)

(c) Averaging processing by time ..... Channel 2 (setting: 1000 msec)

(d) Resolution setting 2 (1/8000)

(3) Devices to be used

(a) Initial setting write command input signal X20

(b) Write data error reset signal.....X21

(c) Digital output value read command input signal.....X22

(d) Write data error occurrence external display.....Y40

(e) Write data error code BCD output .....Y50 to 5B

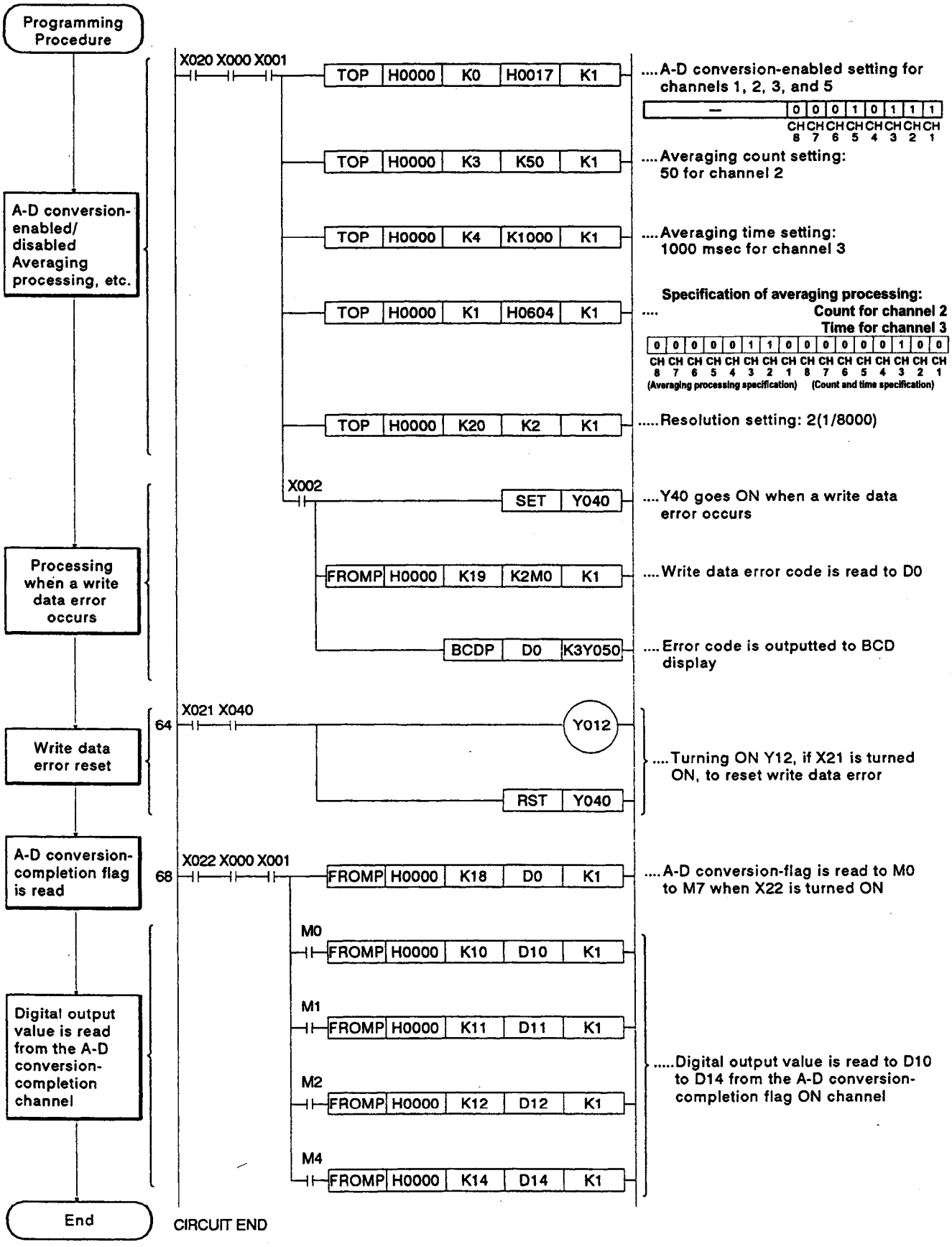
(f) Write data error code storage data register..... D0

(g) A-D conversion-completion flag storage devices..... M0 to M7

(h) Digital output value read destination data registers .....D10 to D14

POINT

During the various processes of the special function modules, the access from the PLC CPU has the priority.
Thus, if the special function module's buffer memory is frequently accessed from the PLC CPU, the scan time of the PLC CPU will increase, and the various processes of the special function module will also be delayed.
Access the buffer memory from the PLC CPU using the FROM/TO commands as necessary.


Programming Procedure
A-D conversion-enabled/ disabled Averaging processing, etc.
Processing when a write data error occurs
Write data error reset
A-D conversion-completion flag is read
Digital output value is read from the A-D conversion-completion channel
End
X020 X000 X001
TOP H0000 K0 H0017 K1
....A-D conversion-enabled setting for channels 1, 2, 3, and 5
CH8 CH7 CH6 CH5 CH4 CH3 CH2 CH1
TOP H0000 K3 K50 K1
....Averaging count setting: 50 for channel 2
TOP H0000 K4 K1000 K1
....Averaging time setting: 1000 msec for channel 3
TOP H0000 K1 H0604 K1
Specification of averaging processing:
Count for channel 2
Time for channel 3
(Averaging processing specification)
(Count and time specification)
TOP H0000 K20 K2 K1
.....Resolution setting: 2(1/8000)
X002
SET Y040
....Y40 goes ON when a write data error occurs
FROMP H0000 K19 K2M0 K1
....Write data error code is read to D0
BCDP D0 K3Y050
....Error code is outputted to BCD display
64
X021 X040
Y012
RST Y040
....Turning ON Y12, if X21 is turned ON, to reset write data error
68
X022 X000 X001
FROMP H0000 K18 D0 K1
....A-D conversion-flag is read to M0 to M7 when X22 is turned ON
M0
FROMP H0000 K10 D10 K1
M1
FROMP H0000 K11 D11 K1
M2
FROMP H0000 K12 D12 K1
M4
FROMP H0000 K14 D14 K1
.....Digital output value is read to D10 to D14 from the A-D conversion-completion flag ON channel
CIRCUIT END

5.2 Sample programs when the A68ADN is mounted onto remote I/O station

[Precautions when writing programs]

(1) Data transmission/receive method

Data transmission/receive is made in the batch refresh mode after executing an END (FEND) instruction, even though the PC CPU I/O control mode is direct or refresh.

(2) Response delay

When transmitting/receiving control information between a master station PC CPU and an A68ADN in a remote I/O station, a response delay is inevitable because control is made through a link module.

Pay attention to control timing.

(3) User instructions

The following instructions are used for data transmission/receive between a master station PC CPU and an A68ADN in a remote I/O station.

(a) Data write (master station → A68ADN): RTOP

(b) Data read (A68ADN → master station): RFRP

(4) Data transmission/receive device

Use link registers (W) for data transmission/receive between a master station PC CPU and an A68ADN in a remote I/O station.

Install the following program to the master station as needed:

(a) When writing data:

Transmit the data that is to be sent the remote I/O station A68ADN to the specified link register before executing an RTOP instruction.

(b) When reading data:

Transmit the link register data to another device before executing an RFRP instruction.

(5) **Simultaneous execution of RTOP and RFRP instructions is not allowed.**

Simultaneous execution of an RTOP instruction and an RFRP instruction at the same time for the same A68ADN cannot be done. Therefore, the data link I/O signal must be added to the program as an interlock condition.

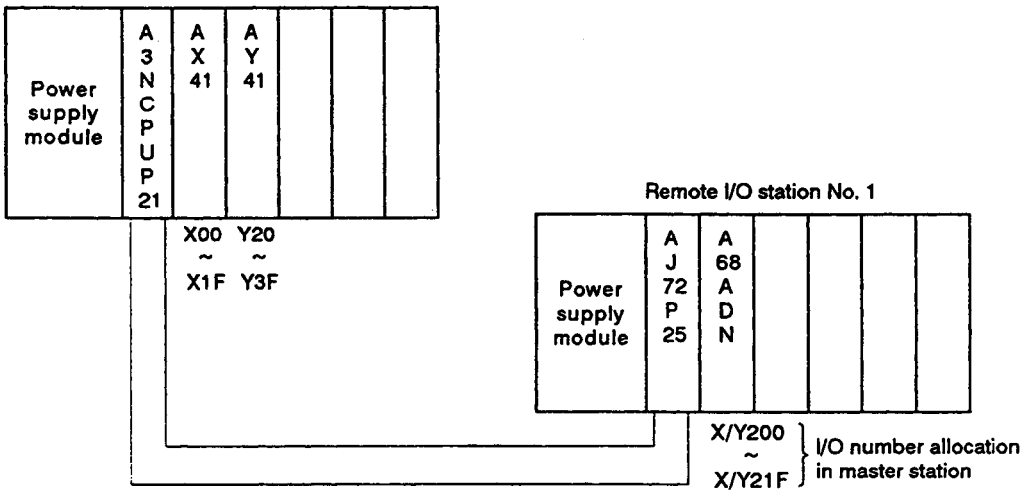
However, if two A68ADNN modules are mounted in a remote I/O station, it is possible to execute an RTOP instruction for one A68ADN and an RFRP instruction for the other module at the same time.

(6) Control signals for the A68ADN

If the output signal (Y[ ][ ] to a remote I/O station is PLS Y[ ][ ]), it may not be output to the A68ADN in accordance with the relationship between the master station scan time and the link scan time.

[Sample Program Conditions]

(1) System configuration



Because the data transmission/receive between a master station and remote I/O station is executed in the batch refresh mode after the execution of an END (FEND) instruction,a pulse output that uses an RST instruction after the execution of the SET instruction cannot be used.

(2) Initial setting

(a) A-D conversion-enabled channel ..... Channels 1, 2, 3, and 5

(b) Averaging processing by count..... **Channel 3 (setting: 50 counts)**

(c) Averaging processing by time ..... Channel 2 (setting: 1000 msec)

(d) Resolution setting 2 (1/8000)

(3) Devices to be used

(a) Intial setting write command input signal X0

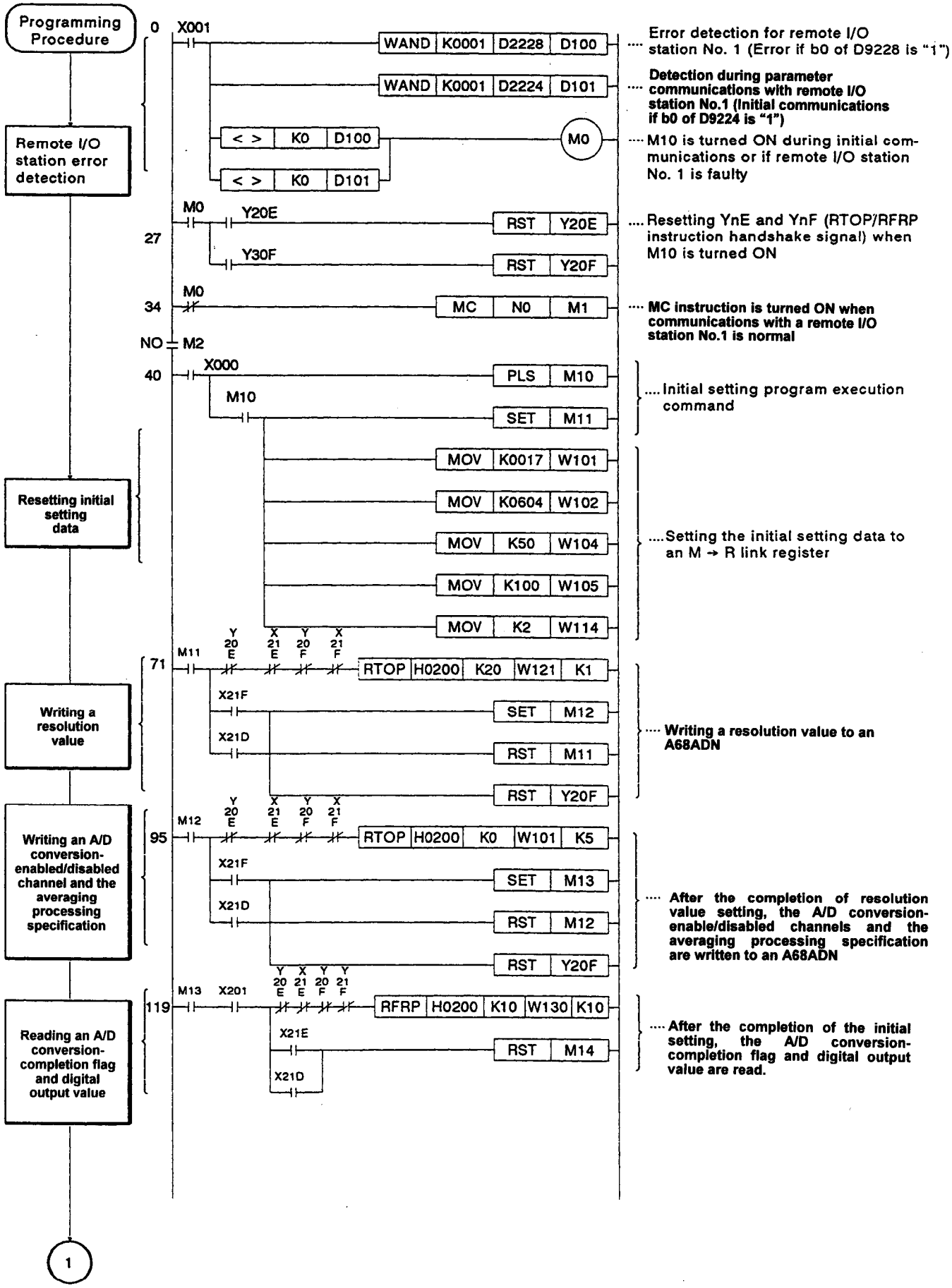
(b) Write data error reset signal..... X2

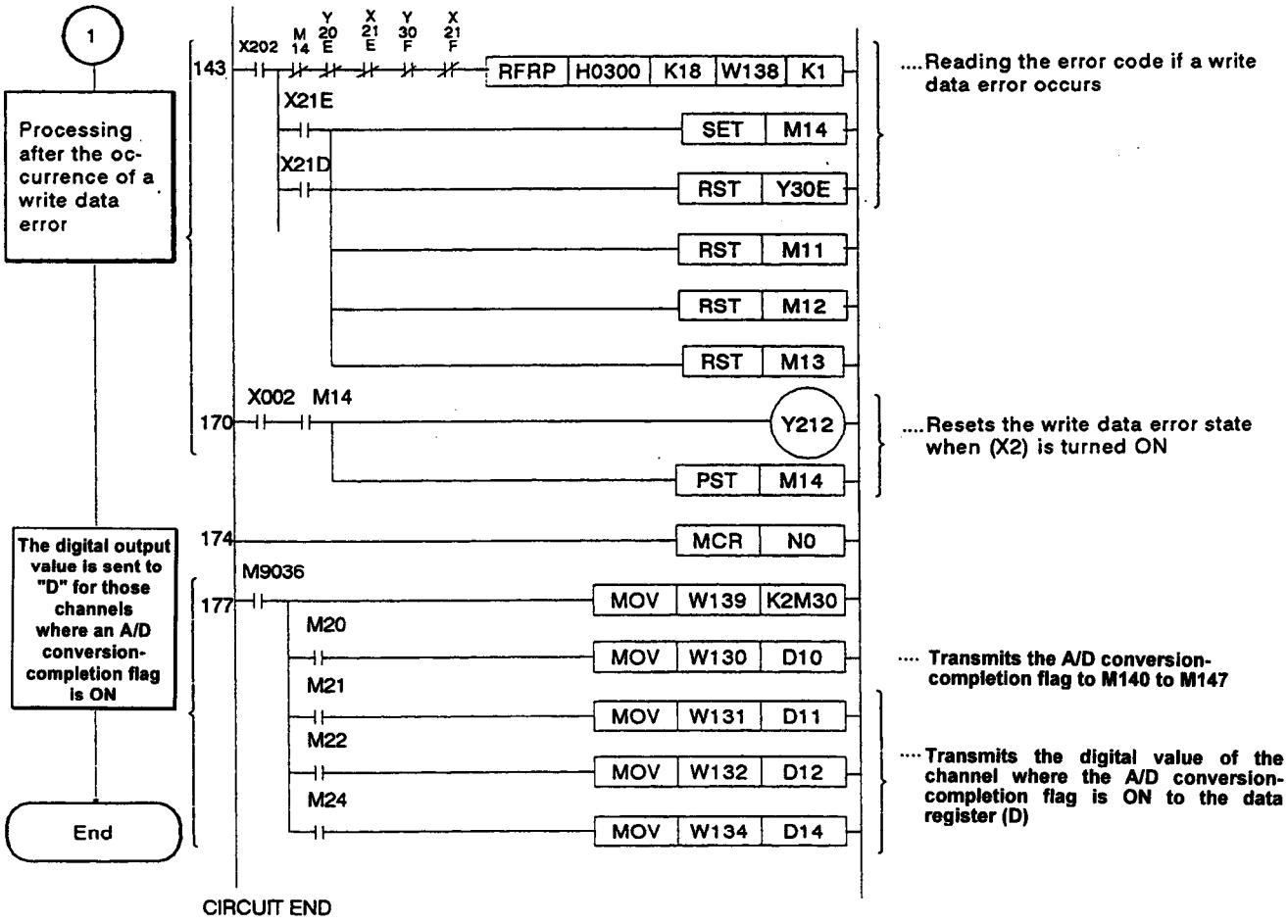
(c) Digital output value read command input signal..... X1

(d) Write data error flag..... Y20

(e) M → R link registers ..... W100 to W12F

(f) R → M link registers ..... W130 to W13F

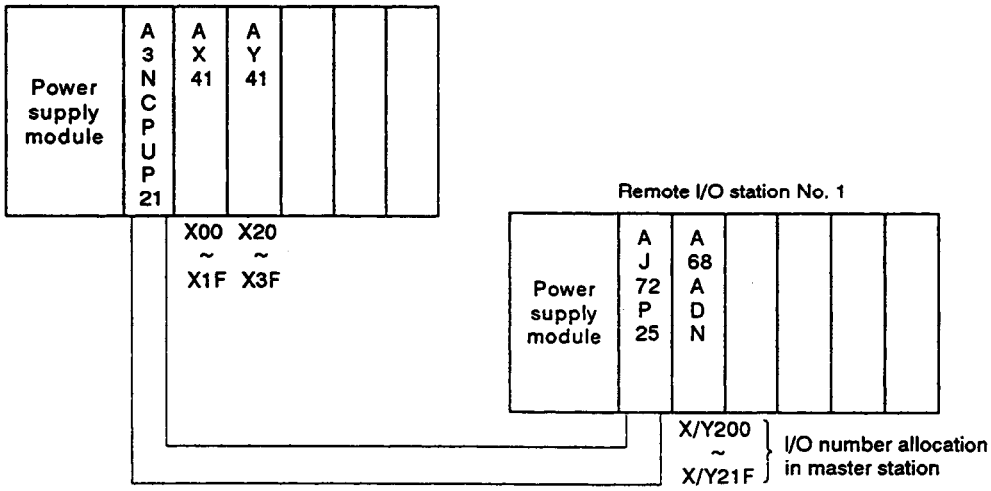

Programming Procedure
Remote I/O station error detection
Resetting initial setting data
Writing a resolution value
Writing an A/D conversion-enabled/disabled channel and the averaging processing specification
Reading an A/D conversion-completion flag and digital output value
0 X001
WAND K0001 D2228 D100
WAND K0001 D2224 D101
< > K0 D100
< > K0 D101
M0
27 M0 Y20E
RST Y20E
Y30F
RST Y20F
34 M0
MC N0 M1
NO = M2
40 X000
PLS M10
M10
SET M11
MOV K0017 W101
MOV K0604 W102
MOV K50 W104
MOV K100 W105
MOV K2 W114
71 M11 Y20E X21E Y20F X21F
RTOP H0200 K20 W121 K1
X21F
SET M12
X21D
RST M11
RST Y20F
95 M12 Y20E X21E Y20F X21F
RTOP H0200 K0 W101 K5
X21F
SET M13
X21D
RST M12
RST Y20F
119 M13 X201 Y20E X21E Y20F X21F
RFRP H0200 K10 W130 K10
X21E
RST M14
X21D
1
Error detection for remote I/O station No. 1 (Error if b0 of D9228 is "1")
Detection during parameter communications with remote I/O station No.1 (Initial communications if b0 of D9224 is "1")
M10 is turned ON during initial communications or if remote I/O station No. 1 is faulty
Resetting YnE and YnF (RTOP/RFRP instruction handshake signal) when M10 is turned ON
MC instruction is turned ON when communications with a remote I/O station No.1 is normal
Initial setting program execution command
Setting the initial setting data to an M → R link register
Writing a resolution value to an A68ADN
After the completion of resolution value setting, the A/D conversion-enable/disabled channels and the averaging processing specification are written to an A68ADN
After the completion of the initial setting, the A/D conversion-completion flag and digital output value are read.


1
Processing after the occurrence of a write data error
The digital output value is sent to "D" for those channels where an A/D conversion-completion flag is ON
End
143
X202
M 14
Y 20 E
X 21 E
Y 30 F
X 21 F
RFRP H0300 K18 W138 K1
X21E
SET M14
X21D
RST Y30E
RST M11
RST M12
RST M13
170
X002 M14
Y212
PST M14
174
MCR N0
M9036
177
MOV W139 K2M30
M20
MOV W130 D10
M21
MOV W131 D11
M22
MOV W132 D12
M24
MOV W134 D14
CIRCUIT END
....Reading the error code if a write data error occurs
....Resets the write data error state when (X2) is turned ON
.... Transmits the A/D conversion-completion flag to M140 to M147
....Transmits the digital value of the channel where the A/D conversion-completion flag is ON to the data register (D)

5.3 Sample programs when the A68ADN is mounted to a remote I/O station (using AnACPU dedicated instructions)

[Sample Program Conditions]

(1) System configuration



(2) Initial setting

(a) A-D conversion-enabled channel ..... Channels 1, 2, 3, and 5

(b) Averaging processing by count .....Channel 3 (setting: 50 times)

(c) Averaging processing by time ..... Channel 2 (setting: 1000 msec)

(d) Resolution setting 2 (1/8000)

(3) Devices to be used

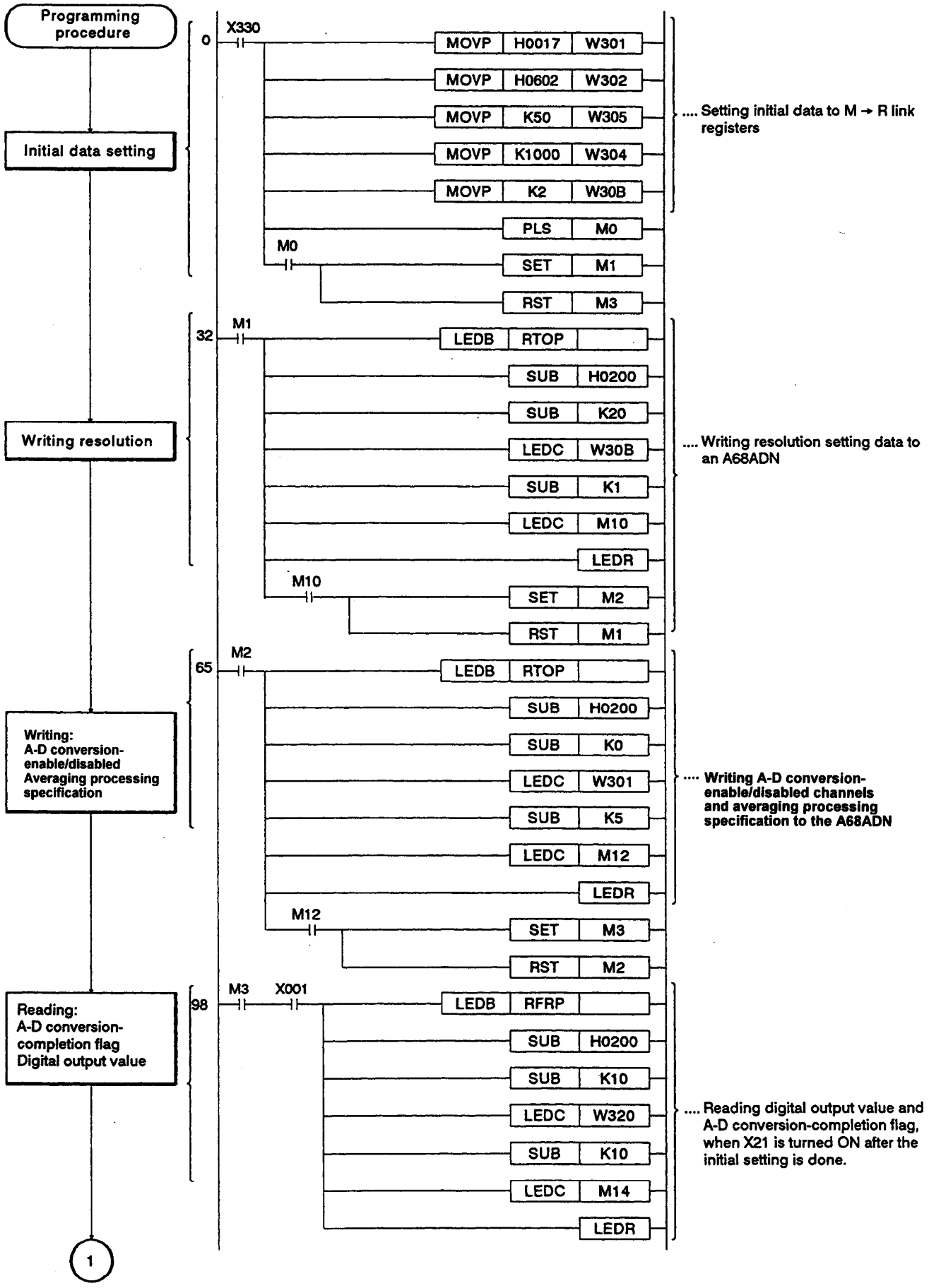
(a) Initial setting write command input signal X20

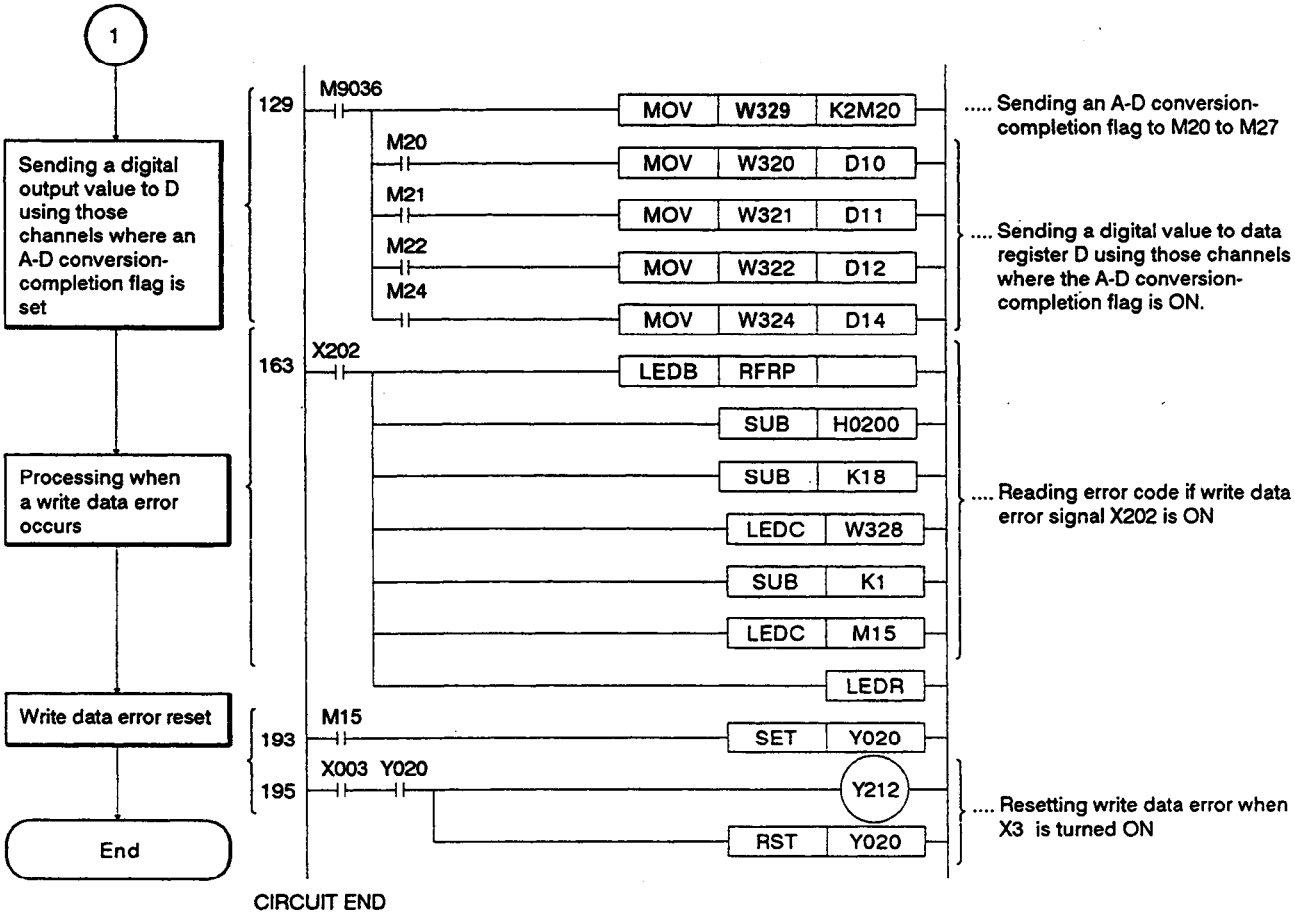
(b) Write data error reset signal.....X23

(c) Digital output value read command input signal.....X21

(d) M → R link registers.....W300 to W31F

(e) R → M link registers.....W320 to W32F


Programming procedure
Initial data setting
Writing resolution
Writing:
A-D conversion-enable/disabled
Averaging processing specification
Reading:
A-D conversion-completion flag
Digital output value
1
0
X330
MOVP H0017 W301
MOVP H0602 W302
MOVP K50 W305
MOVP K1000 W304
MOVP K2 W30B
PLS M0
M0
SET M1
RST M3
.... Setting initial data to M → R link registers
32
M1
LEDB RTOP
SUB H0200
SUB K20
LEDC W30B
SUB K1
LEDC M10
LEDR
M10
SET M2
RST M1
.... Writing resolution setting data to an A68ADN
65
M2
LEDB RTOP
SUB H0200
SUB K0
LEDC W301
SUB K5
LEDC M12
LEDR
M12
SET M3
RST M2
.... Writing A-D conversion-enable/disabled channels and averaging processing specification to the A68ADN
98
M3
X001
LEDB RFRP
SUB H0200
SUB K10
LEDC W320
SUB K10
LEDC M14
LEDR
.... Reading digital output value and A-D conversion-completion flag, when X21 is turned ON after the initial setting is done.


1
Sending a digital output value to D using those channels where an A-D conversion-completion flag is set
Processing when a write data error occurs
Write data error reset
End
129
M9036
MOV W329 K2M20
..... Sending an A-D conversion-completion flag to M20 to M27
M20
MOV W320 D10
M21
MOV W321 D11
M22
MOV W322 D12
M24
MOV W324 D14
.... Sending a digital value to data register D using those channels where the A-D conversion-completion flag is ON.
163
X202
LEDB RFRP
SUB H0200
SUB K18
LEDC W328
SUB K1
LEDC M15
LEDR
.... Reading error code if write data error signal X202 is ON
193
M15
SET Y020
195
X003 Y020
Y212
RST Y020
.... Resetting write data error when X3 is turned ON
CIRCUIT END

MEMO

6. TROUBLESHOOTING

6.1 Error Code List

If an error occurs during PC CPU read/write data operations, the following error codes are stored in the A68ADN buffer memory (address 18).

Table 6.1 Error Code Table (Error Detected by the A68ADN)

Error Code	Causes	Corrective Action
100	• A number other than 1 to 3 is set for resolution setting.	• Set any number of 1 to 30 for resolution setting.
102	• Data is written to the read-only area (addresses 10 to 17)	• Correct the program that specifies the read-only area.
[] 0 to 4	• A value outside the range of 160 to 10000 (msec) is set for averaging time setting. • [ ] indicates the channel where an error is detected. • 0 to 4 : A value in this field has no special meaning. Any number can indicate the averaging time setting error.	• Set the value within the range of 160 to 1000 for averaging time.
[] 5 to 8	• A value outside the range of 1 to 500 (times) is set for averaging count setting. • [ ] indicates the channel where an error is detected. • 5 to 8 : A value in this field has no special meaning. Any number can indicate the averaging count setting error.	• Correct the setting Set the value within the range of 1 to 500 for averaging count.

(1) If more than one type of error occurs, only the error code of the first error is stored in the A68ADN.

(2) To reset the error code, use the sequence program to turn Y12 ON (see Section 5.1).

6.2 Troubleshooting

This section explains the troubleshooting related to the A68ADN. For troubleshooting related to the PC CPU, refer to the appropriate PC CPU User's Manual.

6.2.1 RUN LED (A68ADN) is flashing

Check Point	Corrective Action
Data which disables write or read is written to the A68ADN.	Check the error code table (see Section 6.1) for the cause, and correct the sequence program.

6.2.2 RUN LED (A68ADN) is OFF

Check Point	Corrective Action
Are the TEST terminals open?	After offset/gain setting, open the TEST terminals.
Is the X2 signal (watchdog timer error) ON?	Reset the PC CPU. If the RUN LED is not ON even after the PC CPU is reset, the hardware is faulty. Consult the local Mitsubishi representative.

6.2.3 Digital output value cannot be read

Check Point	Corrective Action
Is the RUN LED (A68ADN) either flashing or OFF?	See Sections 6.2.1 or 6.2.2.
Is the ERROR LED (PC CPU) ON?	See the appropriate PC CPU User's Manual.
Is the RUN LED (PC CPU) either flashing or OFF?	See the appropriate PC CPU User's Manual.
Have conditions to execute a FROM instruction been met?	Monitor the conditions with a peripheral device (like a GPP) to see if they have been met.
Is the buffer memory address specified by a FROM instruction the address for the digital output value from the channel to be read?	Check the sequence program.
Is the channel specified by a FROM instruction A-D conversion enabled?	Read buffer memory address 0 to check the enable/disable setting for the channel in question.
Is A-D conversion completed for the channel specified by a FROM instruction?	Read buffer memory address 19 to see whether or not the A-D conversion-completion flag is set.
Is the analog input signal cable broken or disconnected?	Find the defect, using both visual inspection and a continuity check.
Disconnect the analog input cable from the A68ADN, and apply a test voltage (using either a stabilized power supply or a battery) to measure digital output value.	If the digital output value is correct, it means that the module is influenced by external noise, etc. Check cable connections and grounding.

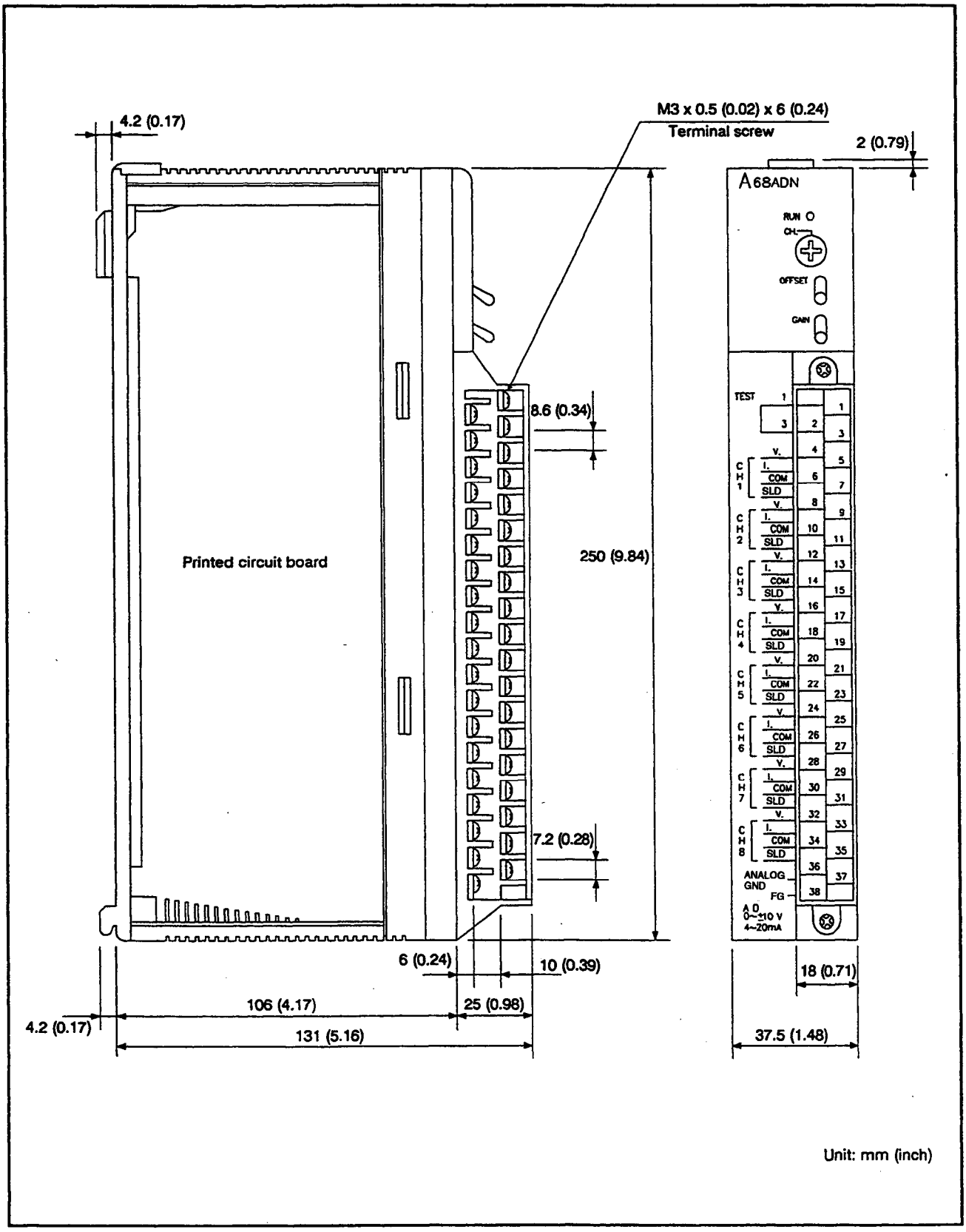
APPENDICES

Appendices1 Comparison of A68ADN and A68AD/A68AD-S2/A616AD Functions

Table A1 Function Comparison

Item		Specifications								
		A68AD	A68AD-S2	A616AD			A68ADN		
Analog input	Voltage	−10 to 0 to 10 VDC (input resistance 30 KΩ)		−10 to 0 to 10 VDC (input resistance 1 MΩ)					
	Current	−20 to 20 mADC (input resistance 250 Ω)							
Digital output	ACPU	16-bit signed binary (−2048 to 2047)		16-bit signed binary (−48 to 4047, −2048 to 2047)			16-bit signed binary (−4096 to 4095, −8192 to 8191, −12288 to 12287)		
	K2ACPU	16-bit signed binary (±2047)		N/A					
Maximum resolution	Voltage	5 mV (1/2000)		1.0 mV (1 to 5 V), 1.25 mV (0 to 5 V), 2.5 mV (0 to 10 V), 5.0 mV (-10 to 10 V)	(1/4000)	Selected with a setting pin	2.5mV 1.25mV 0.83mV	(1/4000) (1/8000) (1/12000)	Selectable
	Current	20 μA (1/1000)		10 μA (0 to 20 mA), 20 μ A (-20 to 20 mA)	(1/2000)	Selected with a setting pin	10mA 5μA 3.3μA	(1/4000) (1/8000) (1/12000)	Selectable
				4 μA (4 to 20 mA), 5 μA (0 to 20 mA), 10 μA (-20 to 20 mA)	(1/4000)				
Overall accuracy		Within ±1%		Within ±6%			Within ±1%		
Maximum conversion speed		Max. 2.5 msec/channel		1 msec/channel			20 msec/channel		
Absolute maximum input	Voltage	±15 V							
	Current	±30 mA							
Number of analog input device points		8 channels/module		16 channels/module (extendable)			8 channels/module		
Conversion method		Scannings per channel							
Offset/gain adjustment		Use offset/gain adjustment knobs		Switched with a setting pin			Use offset/gain adjustment knobs		
Average processing		Enabled		Disabled			Enabled		
Isolation method	Between input terminal and PC CPU	Photocoupler isolation							
	Between channels	Not isolated							
Specification of A-D conversion channel		Set serial channel numbers beginning with CH 1		A-D conversion-enabled/disabled setting					
A-D conversion-completion flag		N/A		When A-D conversion is specified the A-D conversion-completion flag is set, after A-D conversion is completed, and the digital value is written to buffer memory.					

APPENDICES2 External Dimensions



WARRANTY

Please confirm the following product warranty details before starting use.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the dealer or Mitsubishi Service Company. Note that if repairs are required at a site overseas, on a detached island or remote place, expenses to dispatch an engineer shall be charged for.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found to not be the responsibility of Mitsubishi or the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not possible after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of chance loss and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to damages caused by any cause found not to be the responsibility of Mitsubishi, chance losses, lost profits incurred to the user by failures in Mitsubishi products, damages and secondary damages caused from special reasons regardless of Mitsubishi's expectations, compensation for accidents, and compensation for damages to products other than Mitsubishi products and other duties.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.

(2) The Mitsubishi general-purpose programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for each Japan Railways company or the Department of Defense shall be excluded from the programmable logic controller applications.

Note that even with these applications, if the user approves that the application is to be limited and a special quality is not required, application shall be possible.

When considering use in aircraft, medical applications, railways, incineration and fuel devices, manned transport devices, equipment for recreation and amusement, and safety devices, in which human life or assets could be greatly affected and for which a particularly high reliability is required fin terms of safety and control system, please consult with Mitsubishi and discuss the required specifications.

Analog-Digital Converter Module type A68ADN

User's Manual

MODEL	A68ADN-USERS-E
MODEL CODE	13J668
IB(NA)66307-C(0206)MDOC	

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